

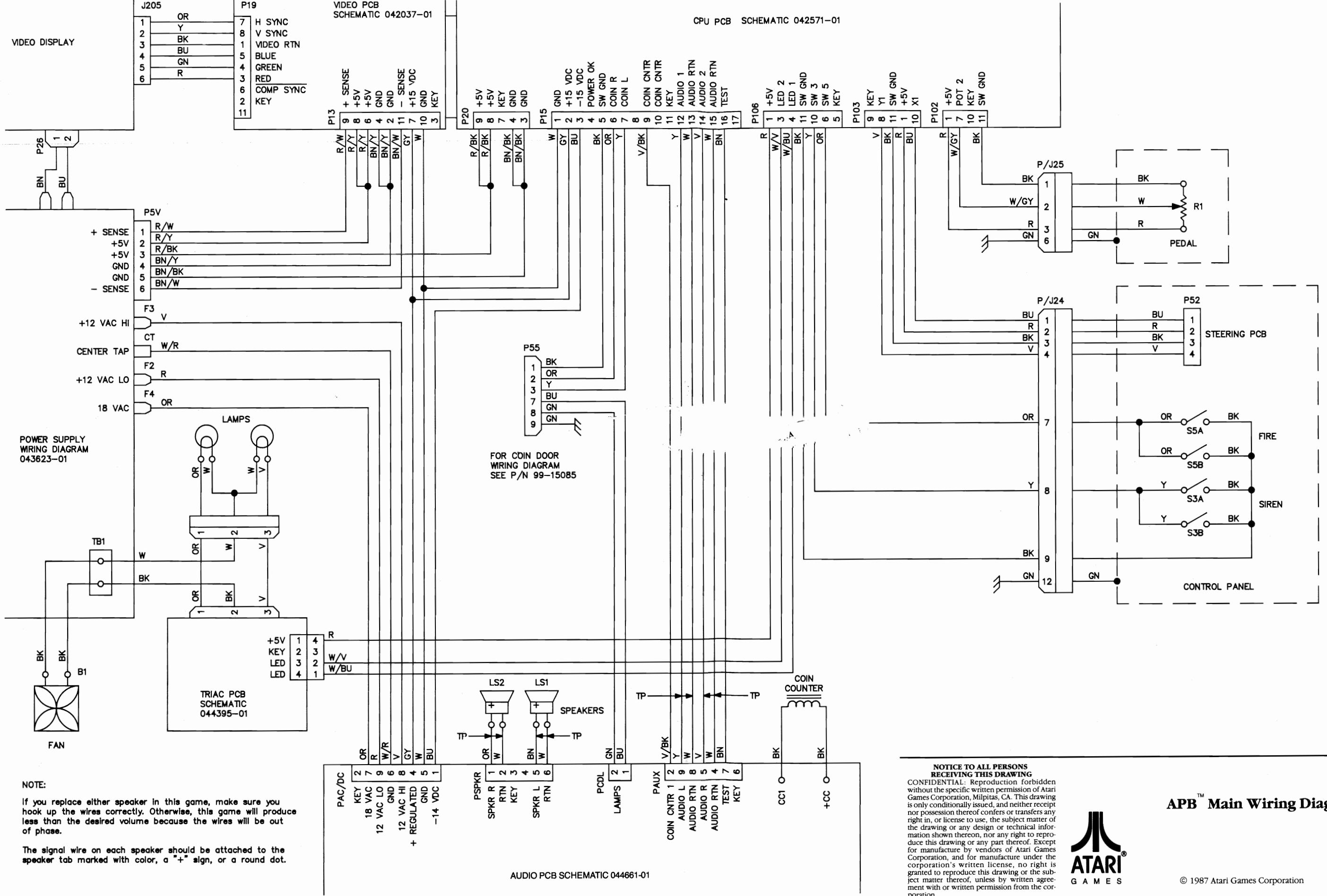
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APB™ Schematic Package

Supplement to the Operators Manual

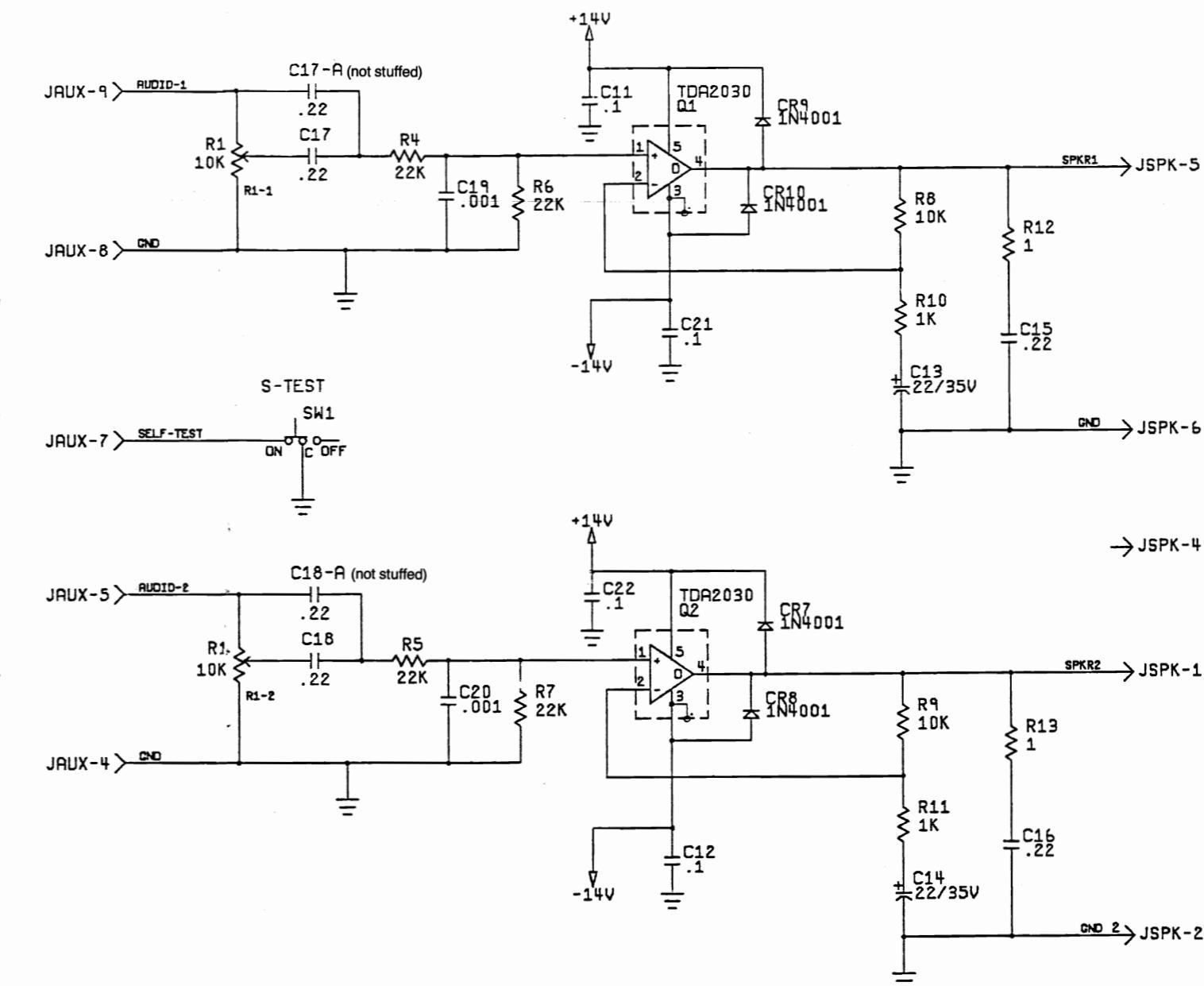
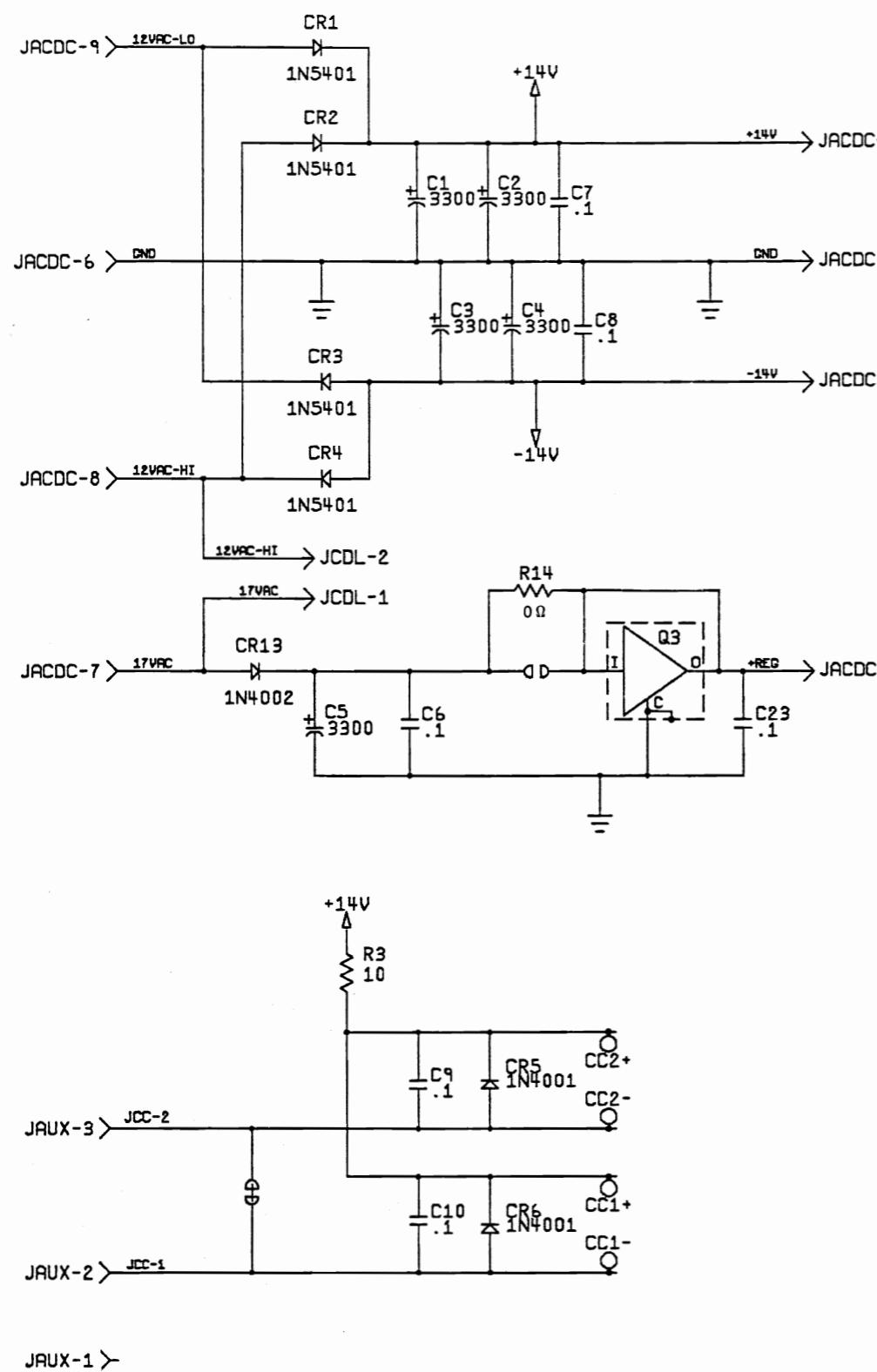




NOTE:

If you replace either speaker in this game, make sure you hook up the wires correctly. Otherwise, this game will produce less than the desired volume because the wires will be out of phase.

The signal wire on each speaker should be attached to the speaker tab marked with color, a "+" sign, or a round dot.



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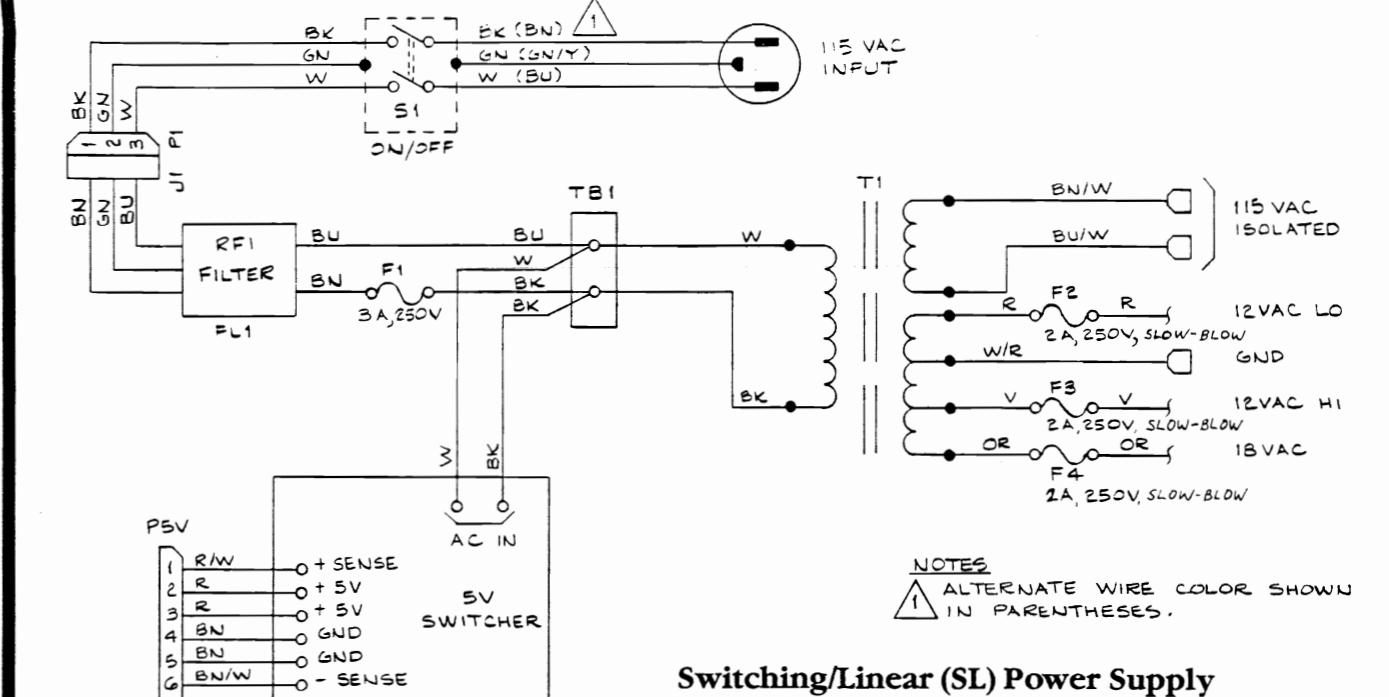
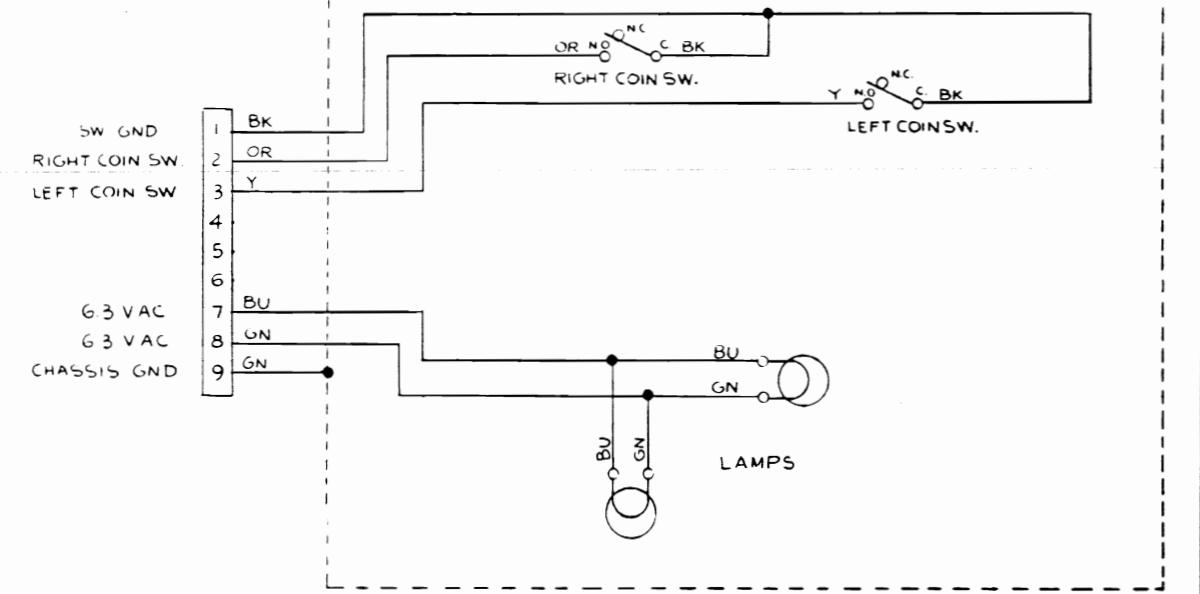
APB™ Audio II
PCB Schematic Diagram



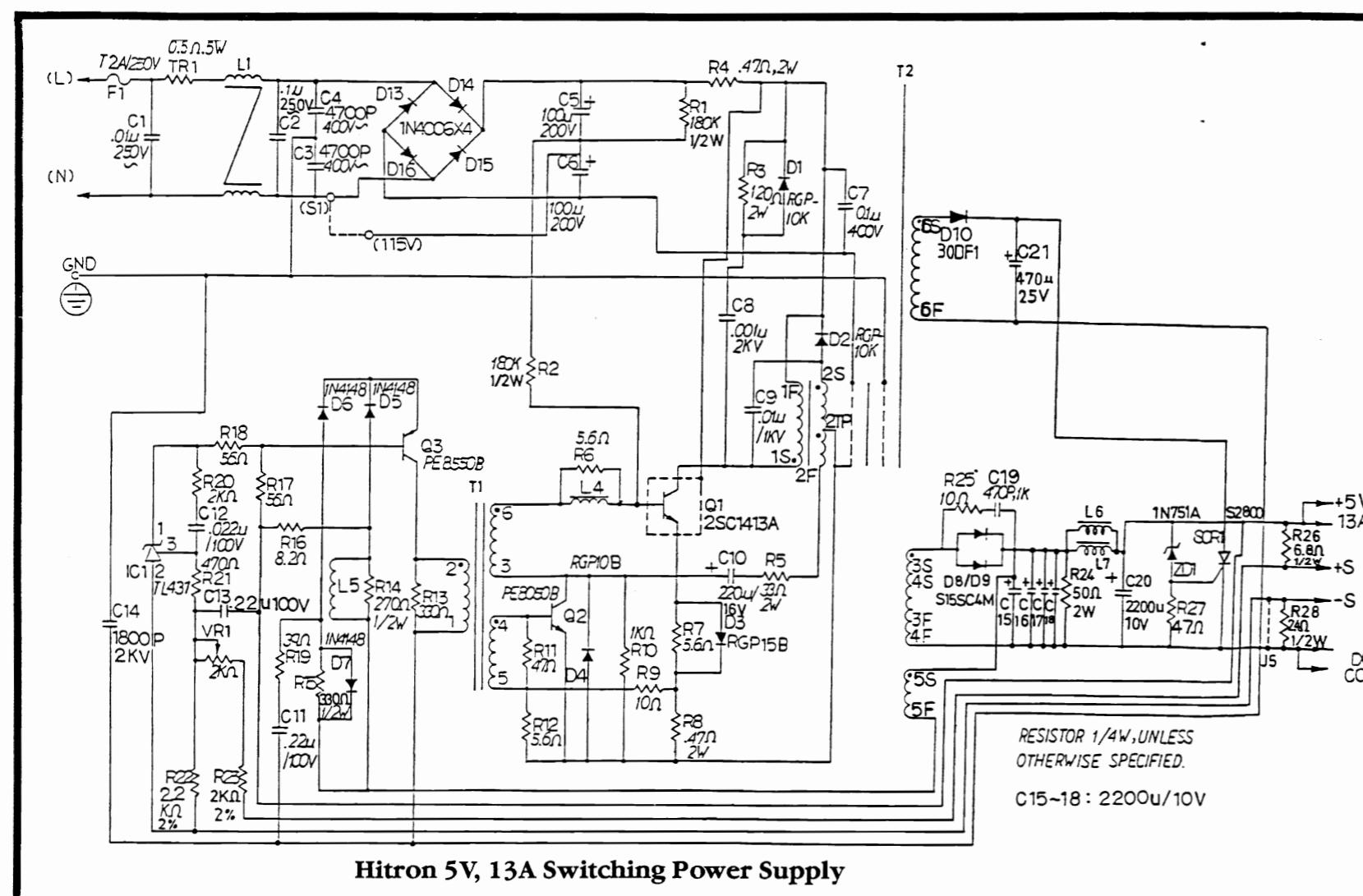
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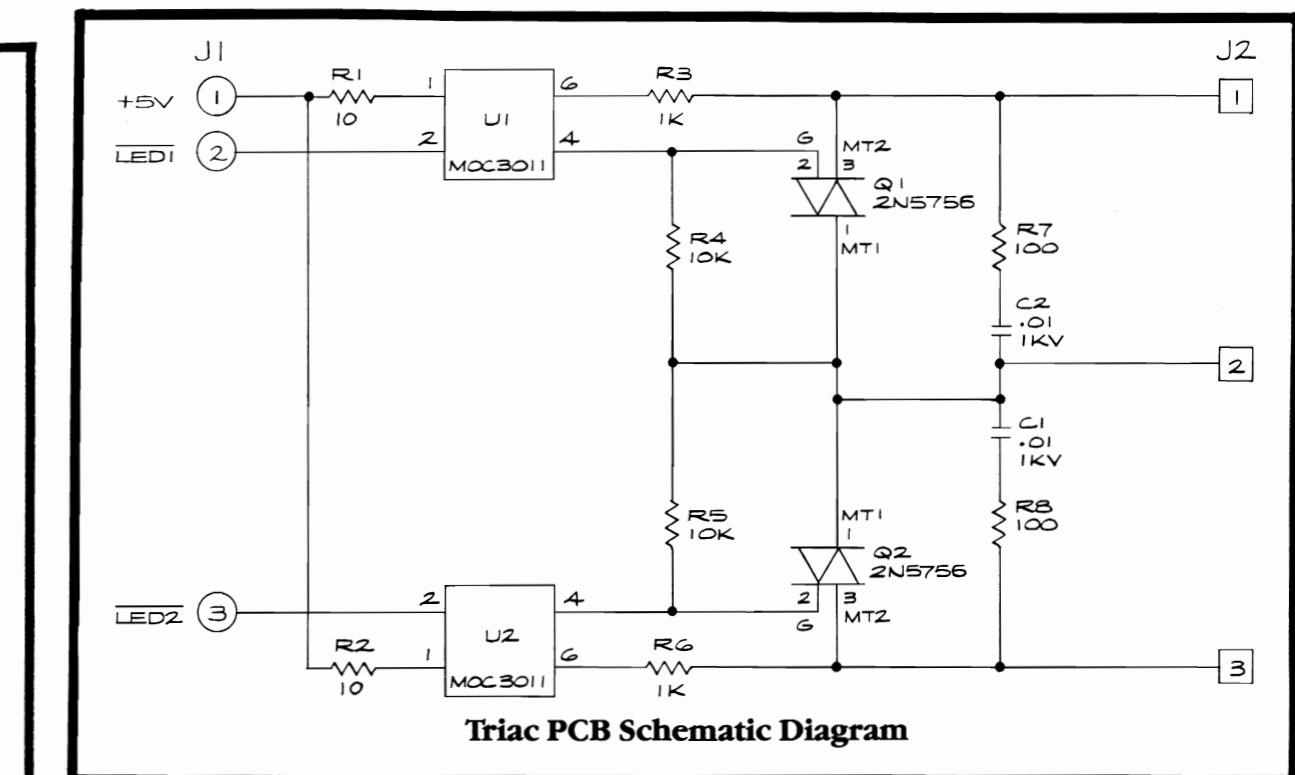
Coin Door Wiring Diagram



Switching/Linear (SL) Power Supply



Hitron 5V, 13A Switching Power Supply



Triac PCB Schematic Diagram

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171027-001

043623-01

149006-001

Main Microprocessor (T-11) Memory Map

Octal	Address Bus Signal Lines			Data Bus Signal Lines			Function and Size
	A	A	A	D	D	D	
000000-007777	0 0 0 0 A A A A A A A A A A A A	R/W	D D D D D D D D D D D D D D D D	Program RAM (4KB)			
010000-010436	0 0 0 1 0 0 A A A A A A A A A O	W	D D D D D D D D D D D D D D D D	Color RAM (144W)			
"	0 0 0 1 0 0 A A A A A A A A A O	W	D D D D D D D D D D D D D D D D	Z (Intensity)			
"	0 0 0 1 0 0 A A A A A A A A A O	W	D D D D D D D D D D D D D D D D	Blue			
"	0 0 0 1 0 0 A A A A A A A A A O	W	D D D D D D D D D D D D D D D D	Green			
"	0 0 0 1 0 0 A A A A A A A A A O	W	D D D D D D D D D D D D D D D D	Red			
010000-010176	0 0 0 1 0 0 0 0 A A A A A A A A A O	W	D D D D D D D D D D D D D D D D	Motion Object Color RAM (64W)			
010200-010276	0 0 0 1 0 0 0 1 A A A A A A A A A O	W	D D D D D D D D D D D D D D D D	Alphanumeric Color RAM (16W)			
010400-010776	0 0 0 1 0 0 1 0 0 A A A A A A A A A O	W	D D D D D D D D D D D D D D D D	Playfield Color RAM (128W)			
012000	0 0 0 1 0 1 0 0 0	O	D D D D D D D D	Program Page 0 Address			
012002	0 0 0 1 0 1 0 0 0	1	D D D D D D D D	Program Page 1 Address			
012200	0 0 0 1 0 1 0 0 1		D D D D D D D D	A/D Converter Start Strobe			
012000-012002	0 0 0 1 0 1 0	A	R	D D D D D D D D	A/D Converter Output		
012400	0 0 0 1 0 1 0 1 0		W	D D	Video Memory Page Select (VMMU)		
012600	0 0 0 1 0 1 0 1 1 0 0		W		IRQ0 Clear		
012640	0 0 0 1 0 1 0 1 1 0 1		W		6502 Reset		
012700	0 0 0 1 0 1 0 1 1 1 0		W		IRQ2 Clear		
012740	0 0 0 1 0 1 0 1 1 1 1		W		IRQ3 Clear		
013000	0 0 0 1 0 1 1 0 0		W	D	IRQ0 Enable 6502 RD (Active High)		
013000	0 0 0 1 0 1 1 0 0		W	D	IRQ1 Enable 6502 WT (Active High)		
013000	0 0 0 1 0 1 1 0 0		W	D	IRQ2 Enable 32V (Active High)		
013000	0 0 0 1 0 1 1 0 0		W	D	IRQ3 Enable VBLANK (Active High)		
013200	0 0 0 1 0 1 1 0 1		W	D D D D D D D D	Communications Port Write		
013400	0 0 0 1 0 1 1 1 0		W	D D D D D D D D D D	Horizontal Scroll & PF Bank 0		
013600	0 0 0 1 0 1 1 1 1		W	D D D D D D D D D D	Vertical Scroll & PF Bank 1		
014000	0 0 0 1 1 0 0 0 0	R		D	SW 6 (Active Low)		
014000	0 0 0 1 1 0 0 0 0	R		D	SW 5 (Active Low)		
014000	0 0 0 1 1 0 0 0 0	R		D	SW 4 (Active Low)		
014000	0 0 0 1 1 0 0 0 0	R		D	SW 3 (Active Low)		
014000	0 0 0 1 1 0 0 0 0	R		D	6502 Comm. Flag (Active High)		
014000	0 0 0 1 1 0 0 0 0	R		D	T-11 Comm. Flag (Active High)		
014000	0 0 0 1 1 0 0 0 0	R		D	SW 2 (Active Low)		
014000	0 0 0 1 1 0 0 0 0	R		D	SW 1 (Active Low)		
014000	0 0 0 1 1 0 0 0 0	R	D		Self-Test (Active Low)		
016000	0 0 0 1 1 1 0 0 0	R	D D D D D D D D	Communications Port Read			
020000-033776	0 0 1 A A A A A A A A A A A A O	R/W	D D D D D D D D D D D D D D D D	Alphanumeric RAM (VMMU=0) (3KW)			
"	0 0 1 A A A A A A A A A A A A O	R/W	D D D D D D D D D D D D D D D D	ANPIC			
034000-037776	0 0 1 1 1 A A A A A A A A A A O	R/W	D D D D D D D D D D D D D D D D	Motion Object RAM (VMMU=0) (1KW)			
"	0 0 1 1 1 A A A A A A A A A O O	R/W	D D D D D D D D D D D D D D D D	MOV			
"	0 0 1 1 1 A A A A A A A A A O 1 0	R/W	D D D D D D D D D D D D D D D D	MOPIC			
"	0 0 1 1 1 A A A A A A A A A A 1 0 0	R/W	D D D D D D D D D D D D D D D D	MOH			
"	0 0 1 1 1 A A A A A A A A A A 1 1 0	R/W	D D D D D D D D D D D D D D D D	MOLNK			
020000-037776	0 0 1 A A A A A A A A A A A A O	R/W	D D D D D D D D D D D D D D D D	Playfield RAM Top (VMMU=2) (4KW)			
020000-037776	0 0 1 A A A A A A A A A A A A O	R/W	D D D D D D D D D D D D D D D D	Playfield RAM Bottom (VMMU=3) (4KW)			
040000-057776	0 1 0 A A A A A A A A A A A A O	R	D D D D D D D D D D D D D D D D	Paged Program (Page 0) (4KW)			
060000-077776	0 1 1 A A A A A A A A A A A A O	R	D D D D D D D D D D D D D D D D	Paged Program (Page 1) (4KW)			
100000-177776	1 A A A A A A A A A A A A O	R	D D D D D D D D D D D D D D D D	Program ROM (16KW)			

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APB™ Main
Microprocessor Memory Map



Sound Microprocessor (6502) Memory Map

Hexa-decimal	A A A A A A A A A A A A A A A A		D D D D D D D D		Function and Size
	1 1 1 1 1 1 0 0 0 0 0 0 0 0 0 0		0 0 0 0 0 0 0 0		
	5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0	R/W	7 6 5 4 3 2 1 0		
0000-0FFF	0 0 0 0 A A A A A A A A A A A A	R/W	D D D D D D D D		Program RAM (4KB)
1000-17FF	0 0 0 1 0 A A A A A A A A A A A A	R/W	D D D D D D D D		EEROM (2KB)
1800-180F	0 0 1 1 0 0 0 A A A A A A A A	R/W	D D D D D D D D		POKEY 1 (16B)
1810-1813	0 0 1 1 0 0 1 A A A A A A A A	R	D D D D D D D D		LETA
1830-183F	0 0 1 1 0 1 1 A A A A A A A A	R/W	D D D D D D D D		POKEY 2 (16B)
1840	0 0 1 1 1 0 0 A A A A A A A A	R		D	T-11 Talk (Active High)
1840	0 0 1 1 1 0 0 A A A A A A A A	R		D	6502 Talk (Active High)
1840	0 0 1 1 1 0 0 A A A A A A A A	R		D	TI READY (Active High)
1840	0 0 1 1 1 0 0 A A A A A A A A	R		D	
1840	0 0 1 1 1 0 0 A A A A A A A A	R		D	Self-Test Switch (Active Low)
1840	0 0 1 1 1 0 0 A A A A A A A A	R		D	Auxiliary Coin Switch (Active Low)
1840	0 0 1 1 1 0 0 A A A A A A A A	R		D	Left Coin Switch (Active Low)
1840	0 0 1 1 1 0 0 A A A A A A A A	R		D	Right Coin Switch (Active Low)
1850-1851	0 0 1 1 1 0 1 A A A A A A A A	R	D D D D D D D D		Yamaha Sound Chip
1860	0 0 1 1 1 1 0 A A A A A A A A	R	D D D D D D D D		Communications Port Read
1870	0 0 1 1 1 1 1 0 0 0 A A A A A A	W	D D D D D D D D		TI Data
1872-1873	0 0 1 1 1 1 1 0 0 1 A A A A A A	W	D D D D D D D D		TI Write Enable
1874	0 0 1 1 1 1 1 0 1 0 A A A A A A	W	D D D D D D D D		Communications Port Write
1876	0 0 1 1 1 1 1 0 1 1 A A A A A A	W		D	Right Coin Counter (Active High)
1876	0 0 1 1 1 1 1 0 1 1 A A A A A A	W		D	Left Coin Counter (Active High)
1878	0 0 1 1 1 1 1 1 0 0 A A A A A A	W			IRQ Clear
187A	0 0 1 1 1 1 1 1 0 1 A A A A A A	W		D D D	Yamaha Mixer
187A	0 0 1 1 1 1 1 1 0 1 A A A A A A	W		D D	POKEY Mixer
187A	0 0 1 1 1 1 1 1 0 1 A A A A A A	W		D D D	TI Sound Mixer
187C	0 0 1 1 1 1 1 1 1 0 A A A A A A	W		D	LED 1
187C	0 0 1 1 1 1 1 1 1 0 A A A A A A	W		D	LED 2
187C	0 0 1 1 1 1 1 1 1 0 A A A A A A	W		D	LETA Resolution
187C	0 0 1 1 1 1 1 1 1 0 A A A A A A	W		D	TI Frequency Select
187E	0 0 1 1 1 1 1 1 1 1 A A A A A A	W		D	Sound Enable (Active High)
4000-7FFF	0 1 A A A A A A A A A A A A A A A A	R	D D D D D D D D		Program ROM (16KB)
8000-FFFF	1 A A A A A A A A A A A A A A A A	R	D D D D D D D D		Program ROM (32KB)

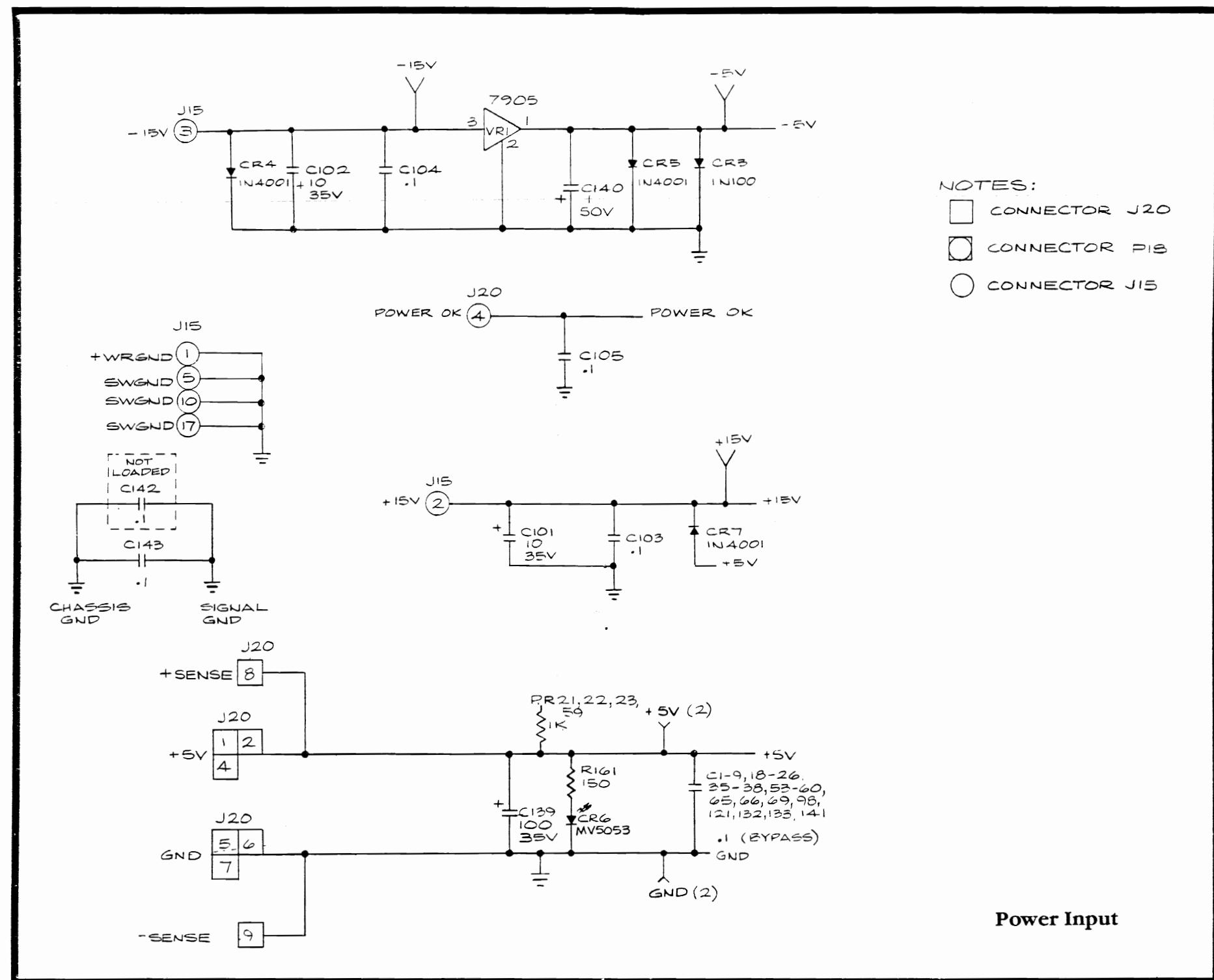
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APB™ Sound
Microprocessor Memory Map



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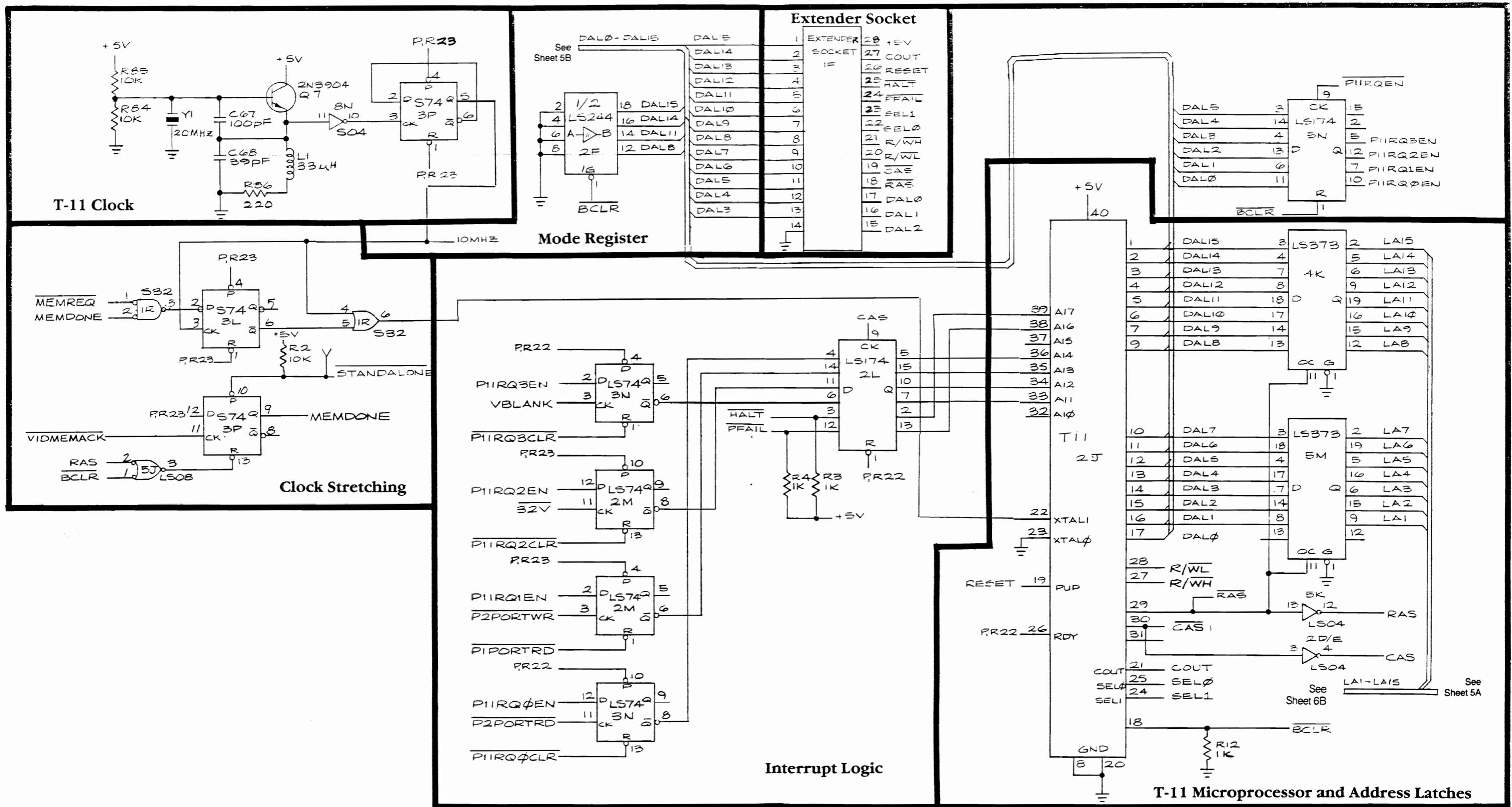
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**APB™ CPU PCB
Schematic Diagram**



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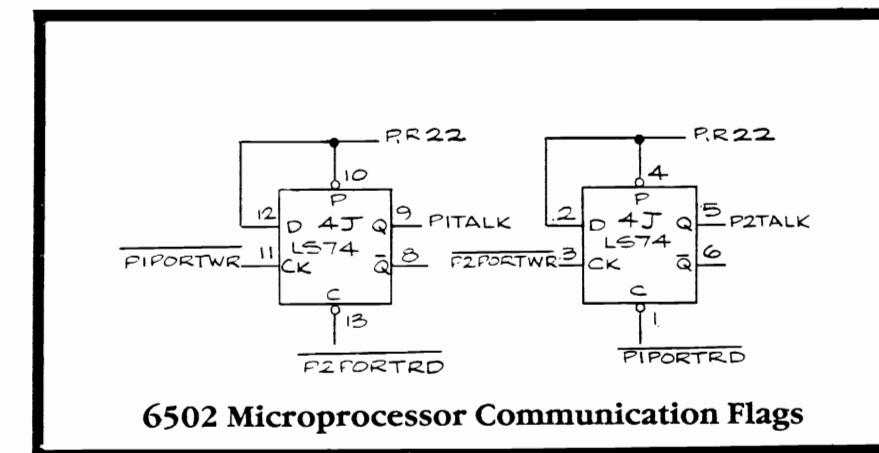
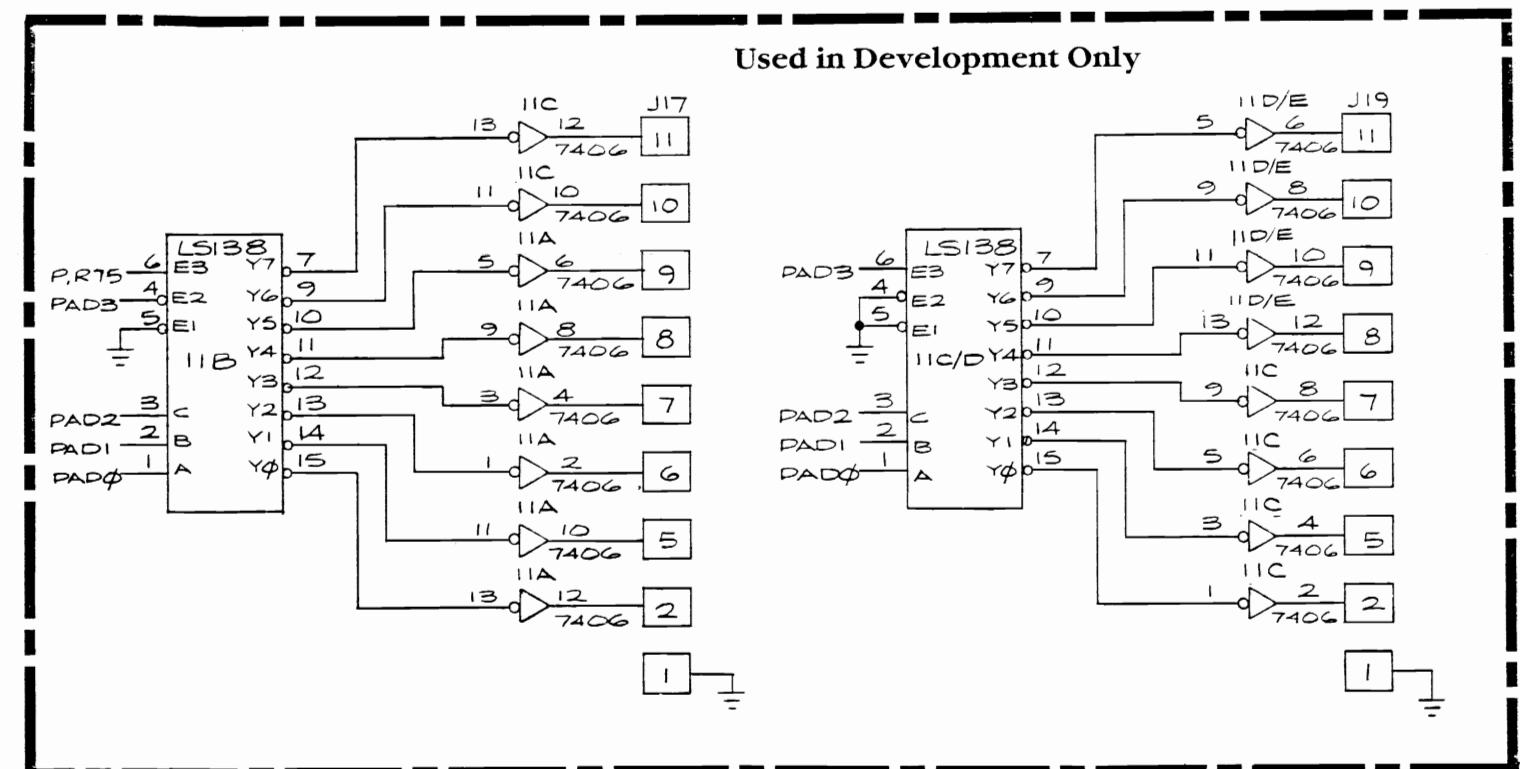
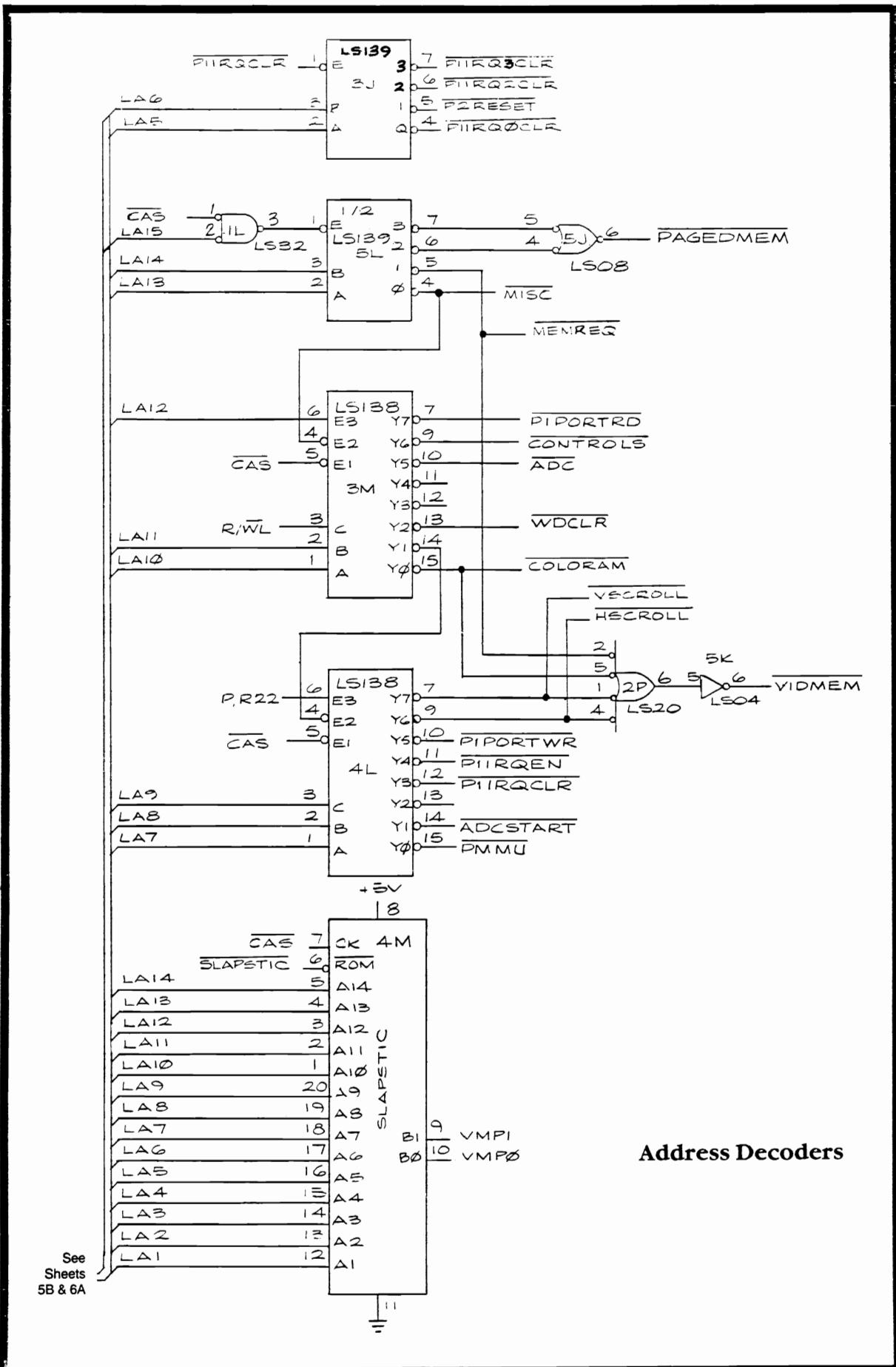
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APB™ CPU PCB
Schematic Diagram



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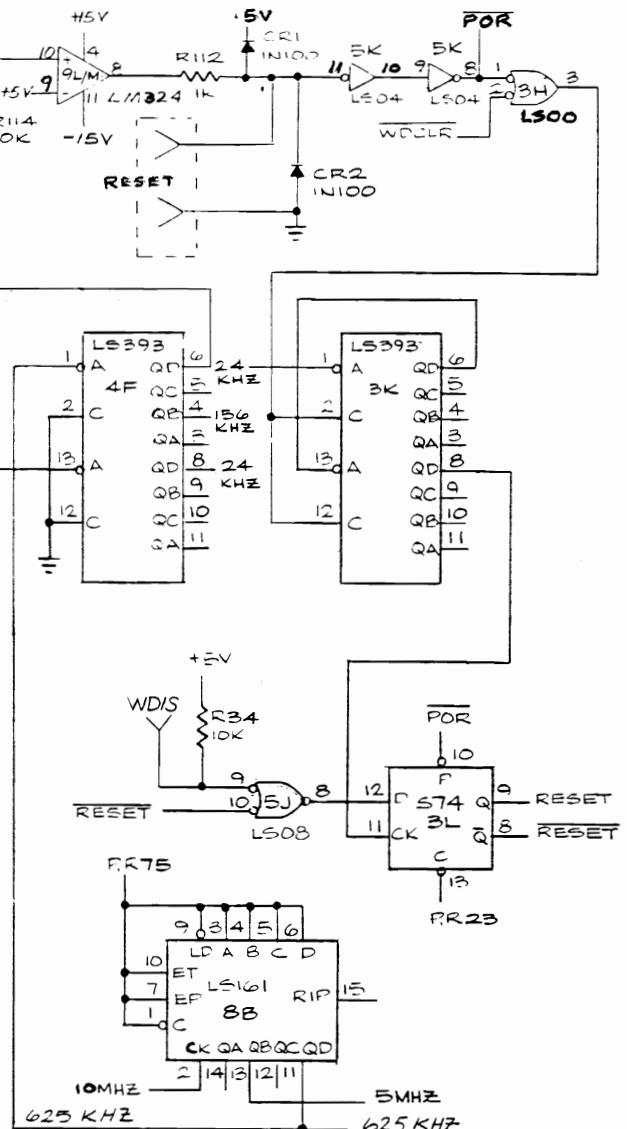
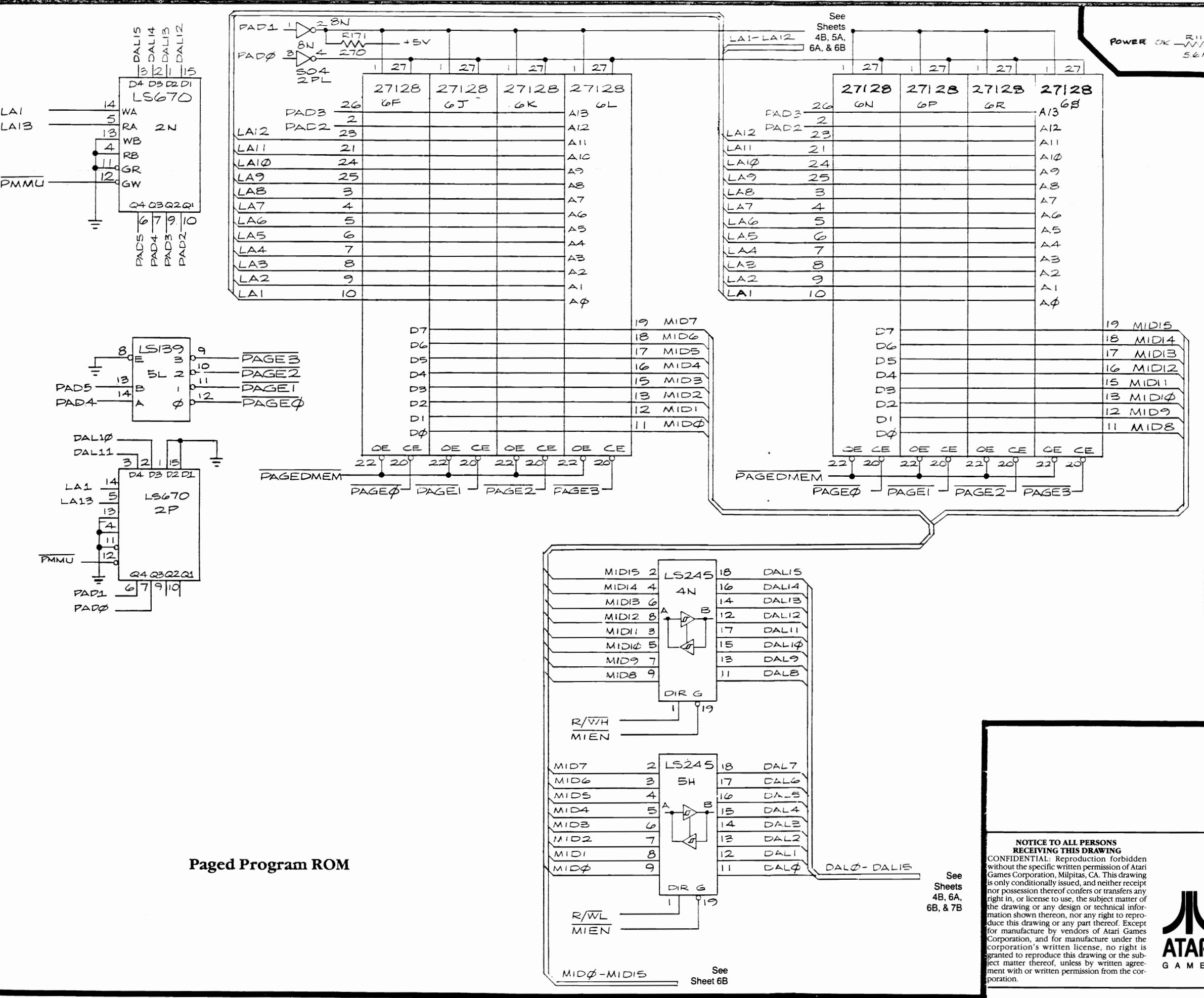
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APB™ CPU PCB
Schematic Diagram





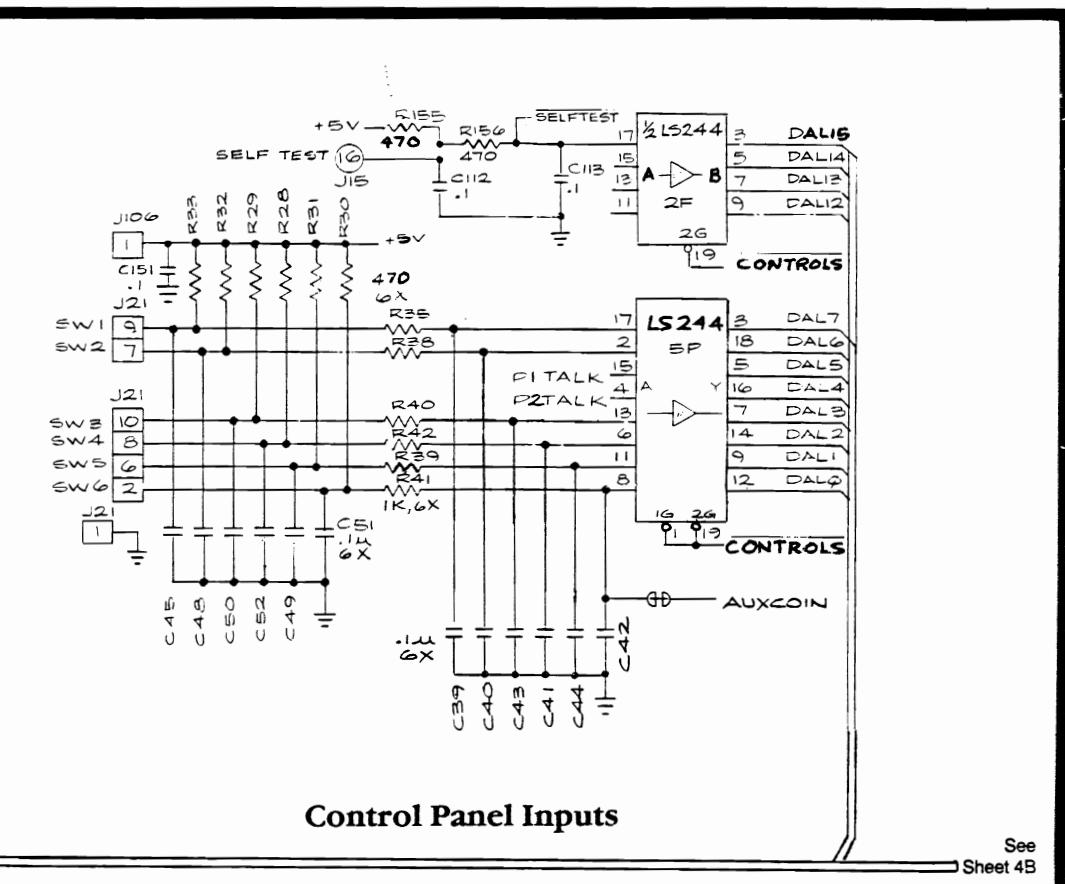
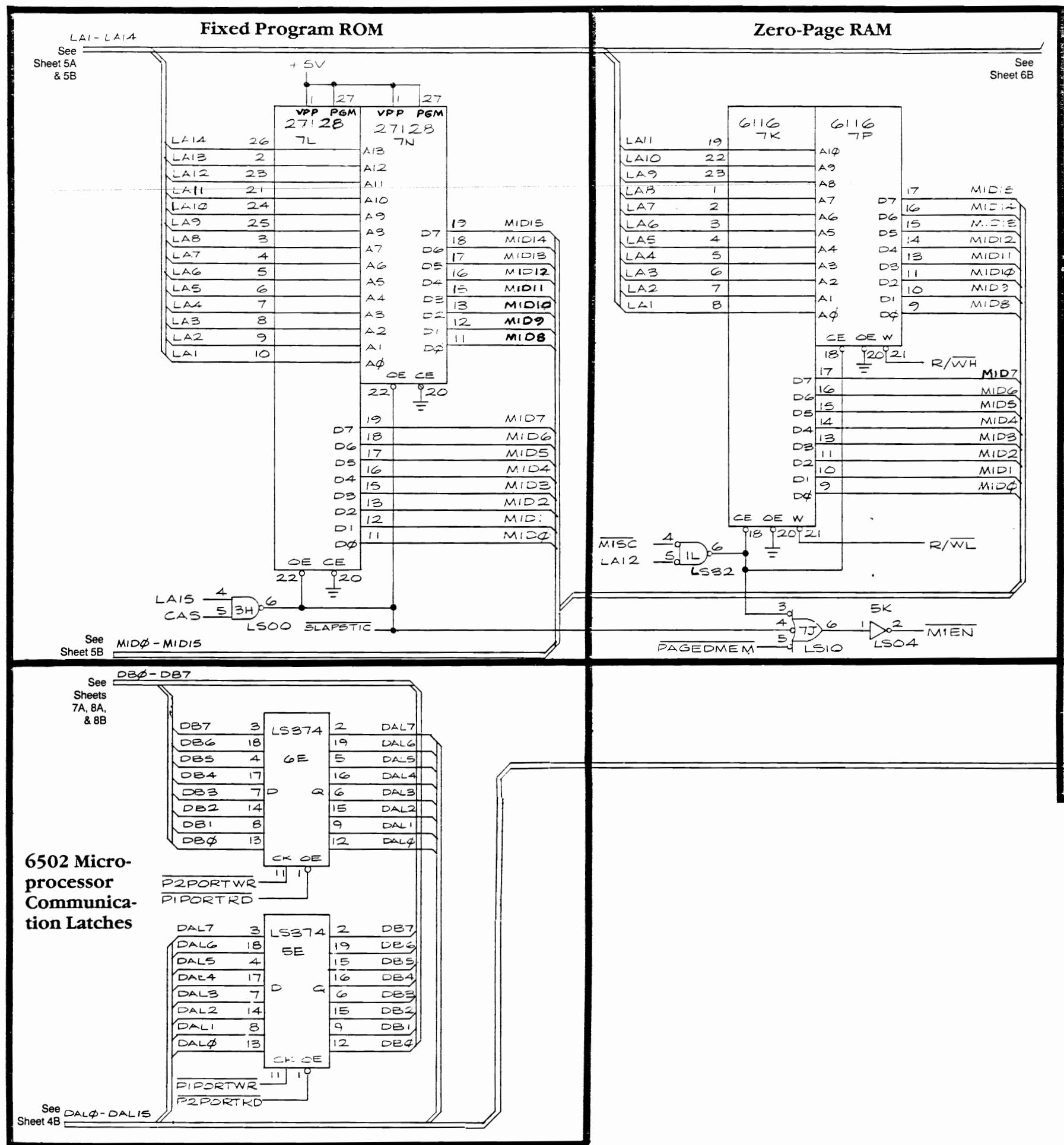
Reset and Watchdog Clear

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APB™ CPU PCB Schematic Diagram



6502 Micro-processor Communication Latches

See DALφ - DALIS
Sheet 4B

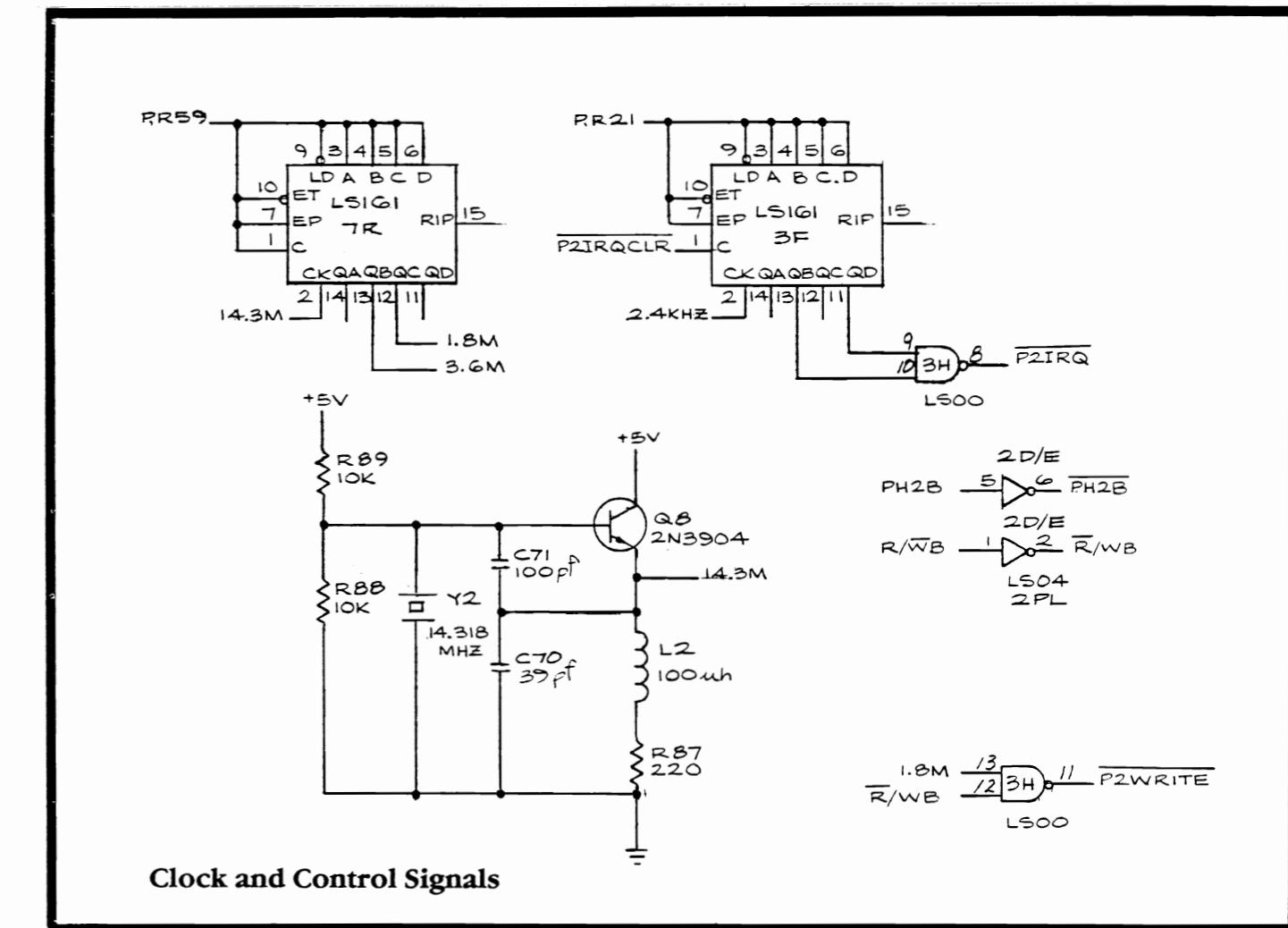
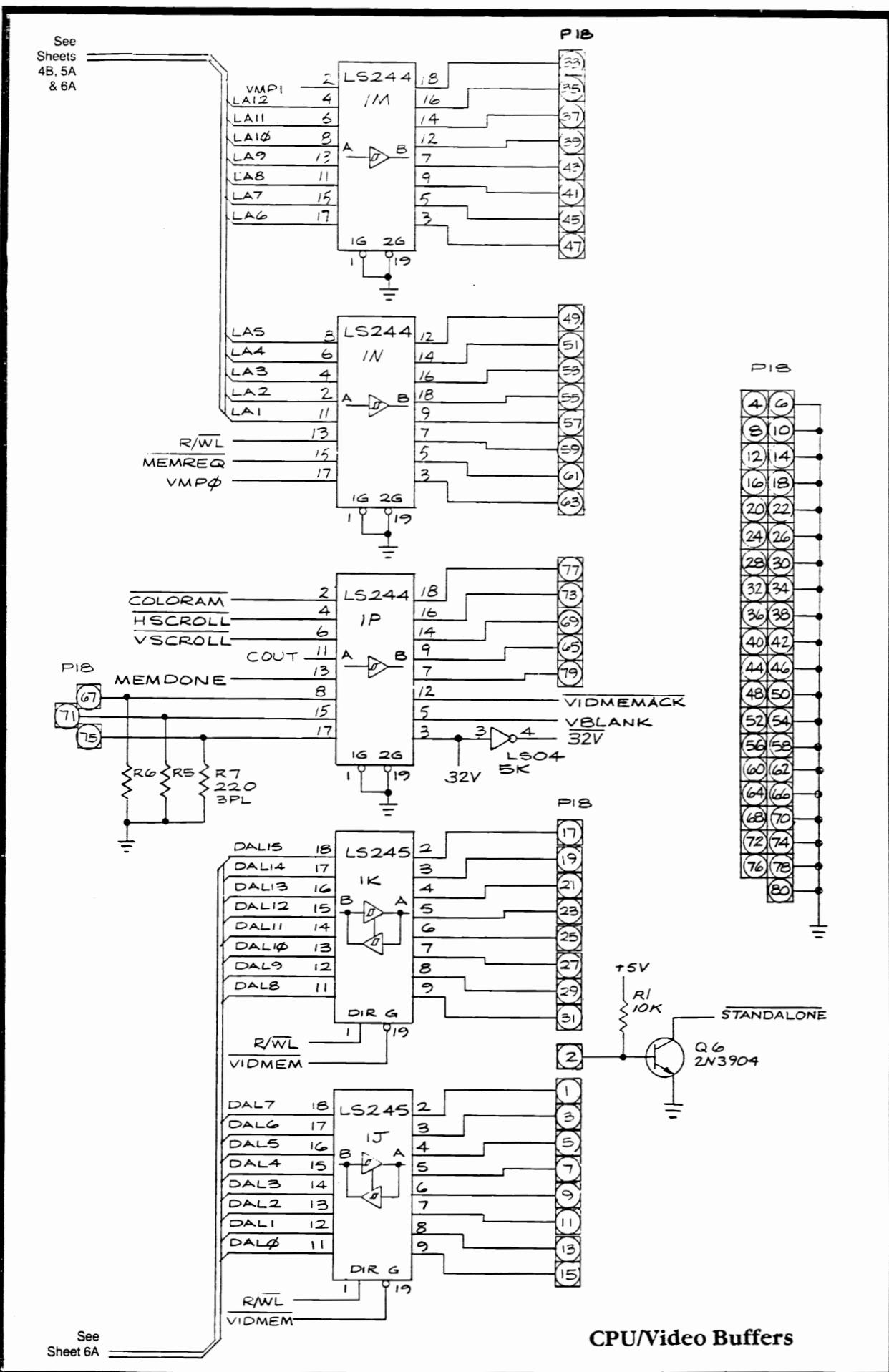
Control Panel Inputs

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APB™ CPU PCB

Schematic Diagram





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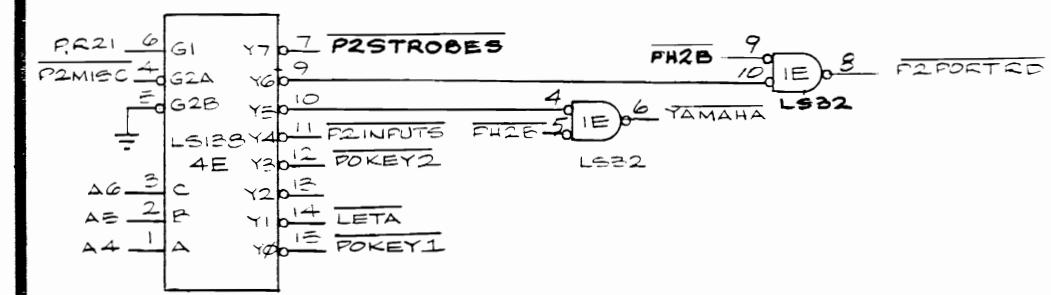
**APB™ CPU PCB
Schematic Diagram**



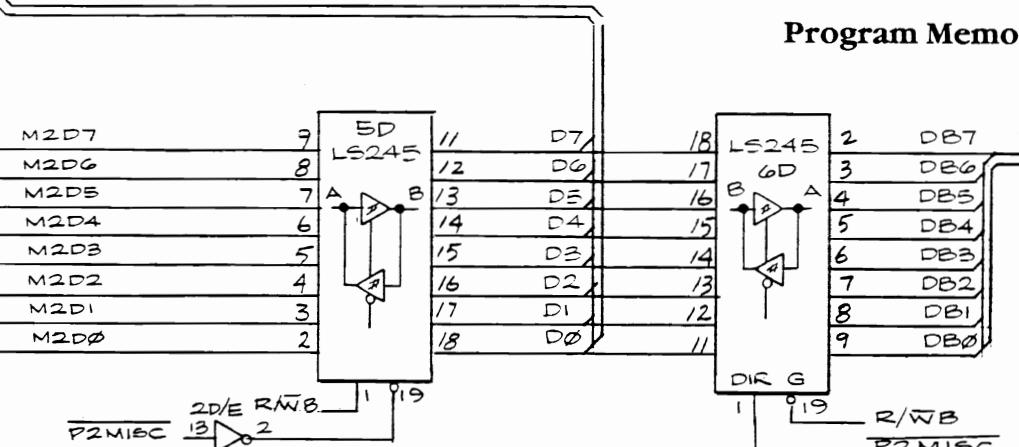
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Address Decoding

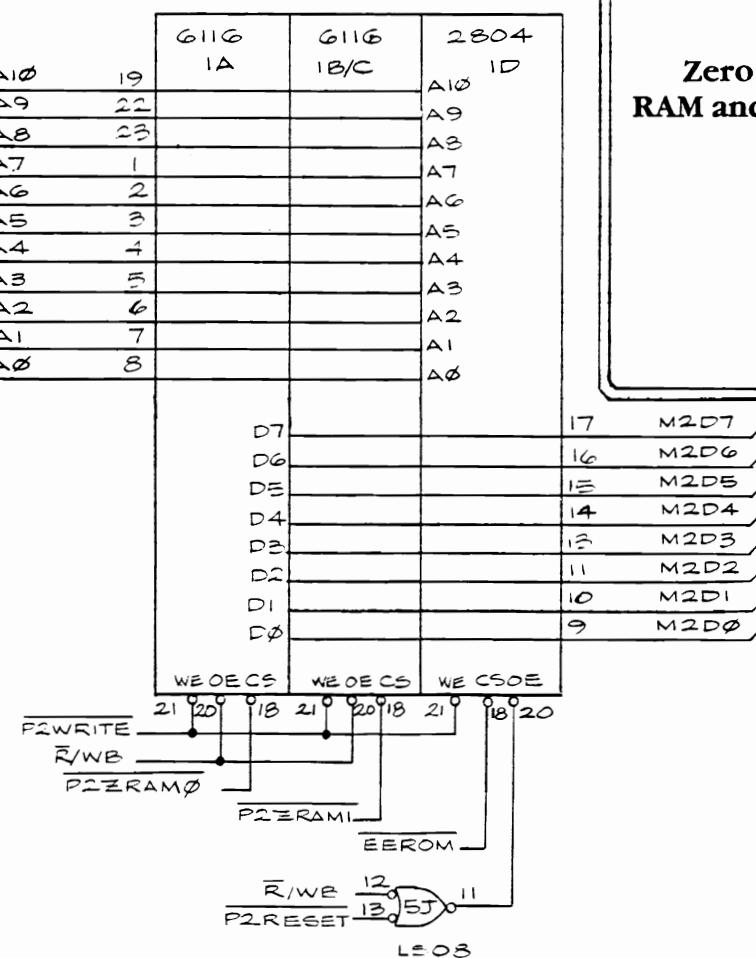


Program Memory



See
Sheets
6A, 8A,
& 8B

Zero Page RAM and EEPROM

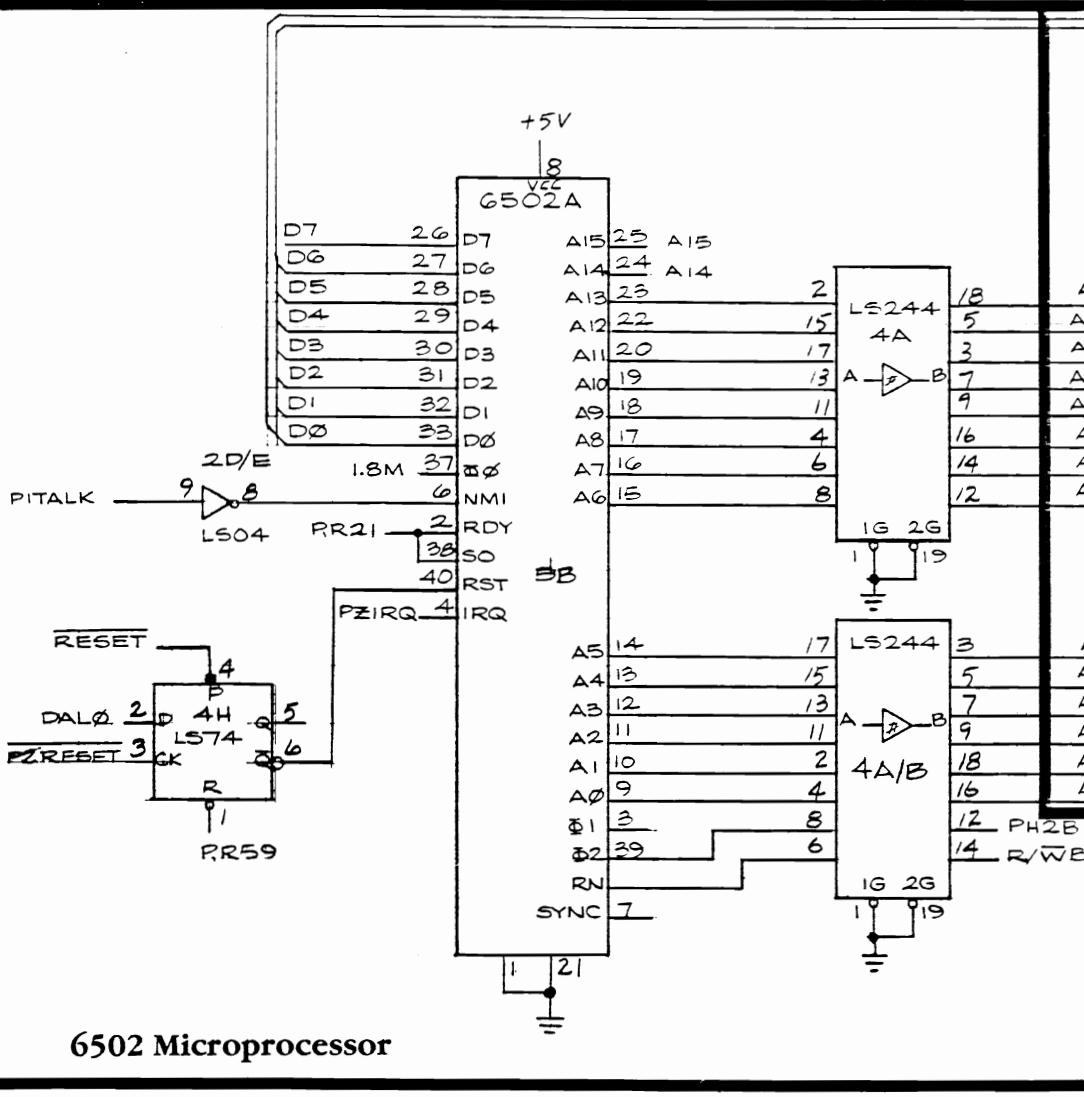


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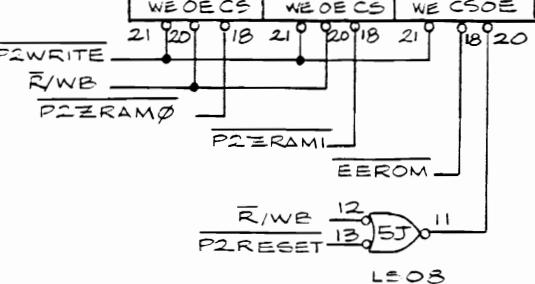
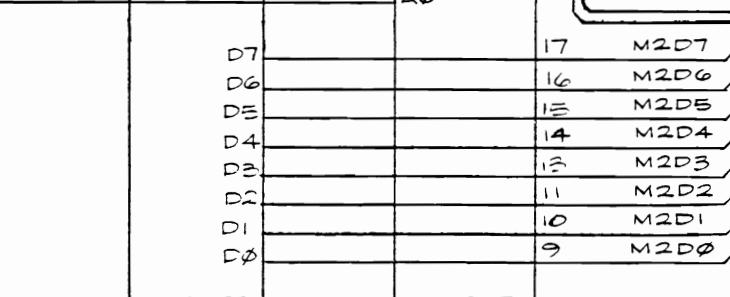
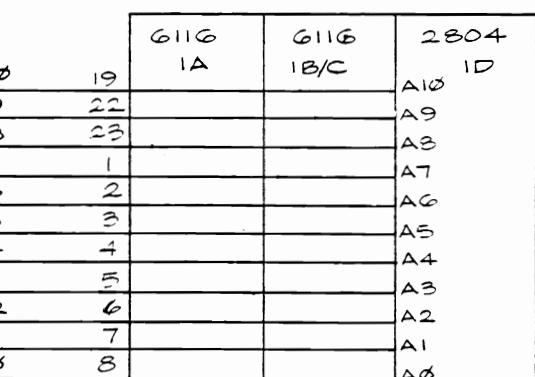
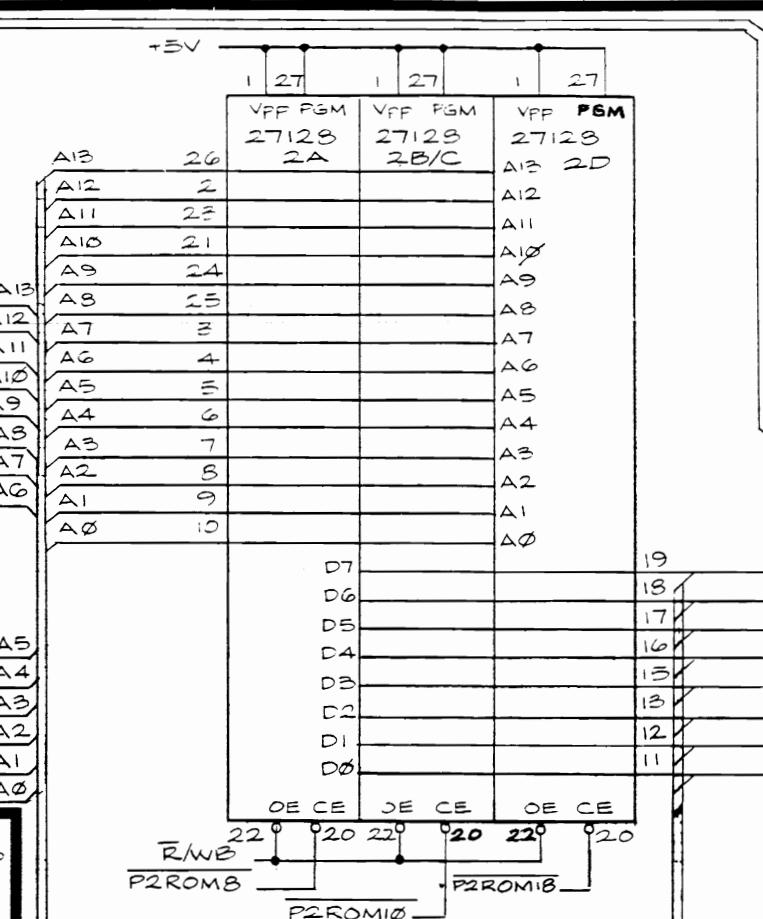
APB™ CPU PCB Schematic Diagram



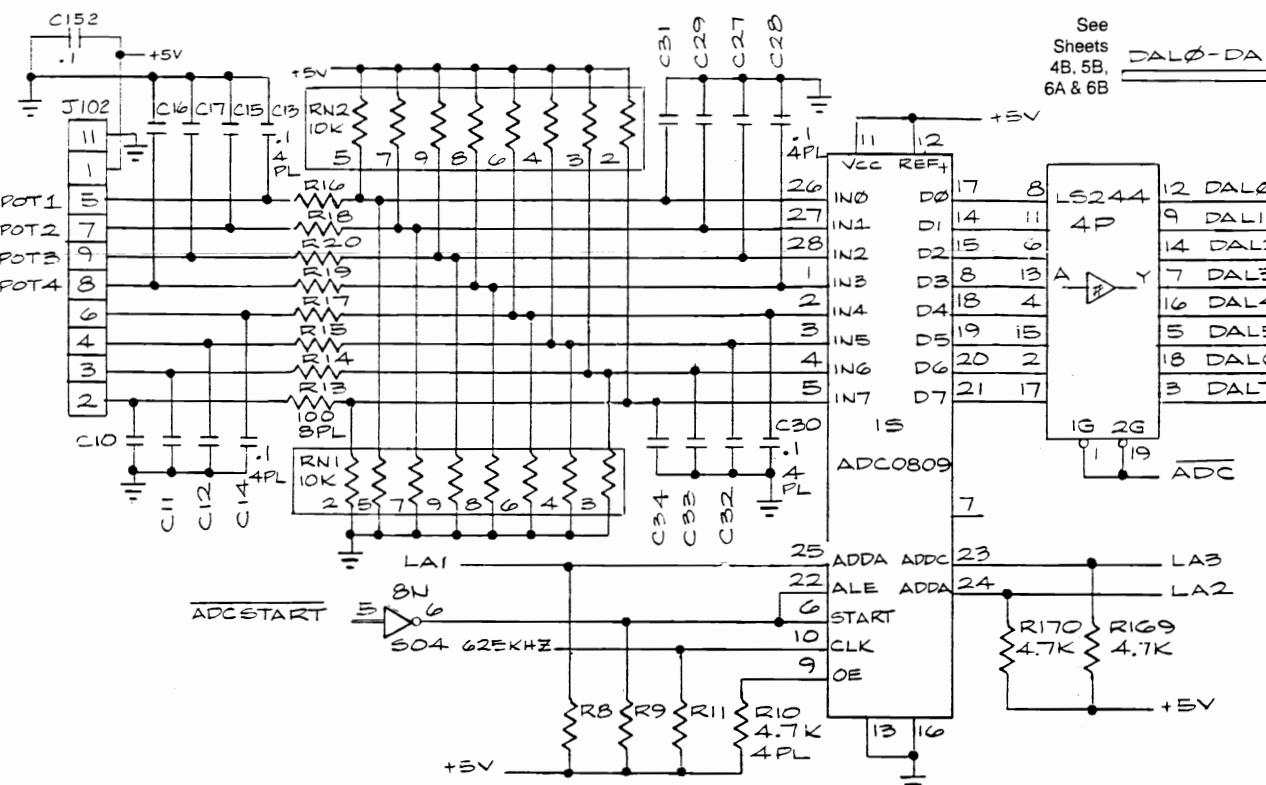
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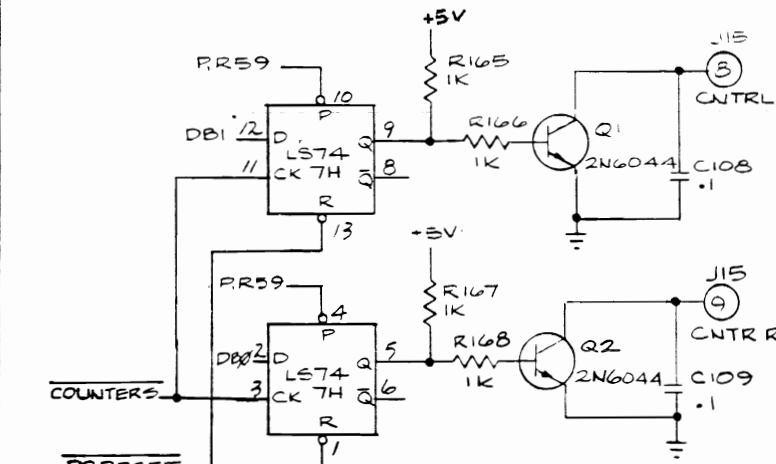
6502 Microprocessor



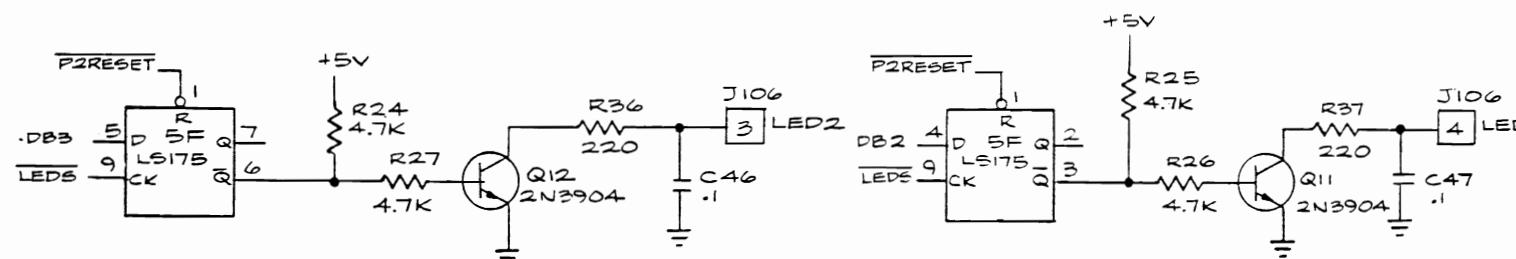
A/D Converter



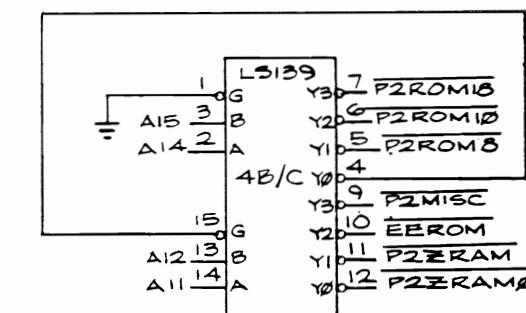
Coin Counters



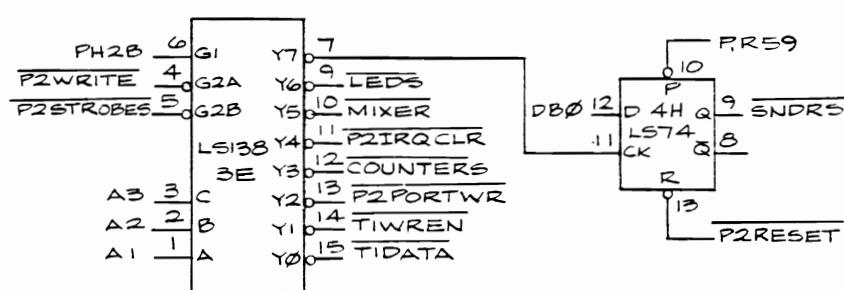
LED Drivers



Address Decoding



Address Decoding

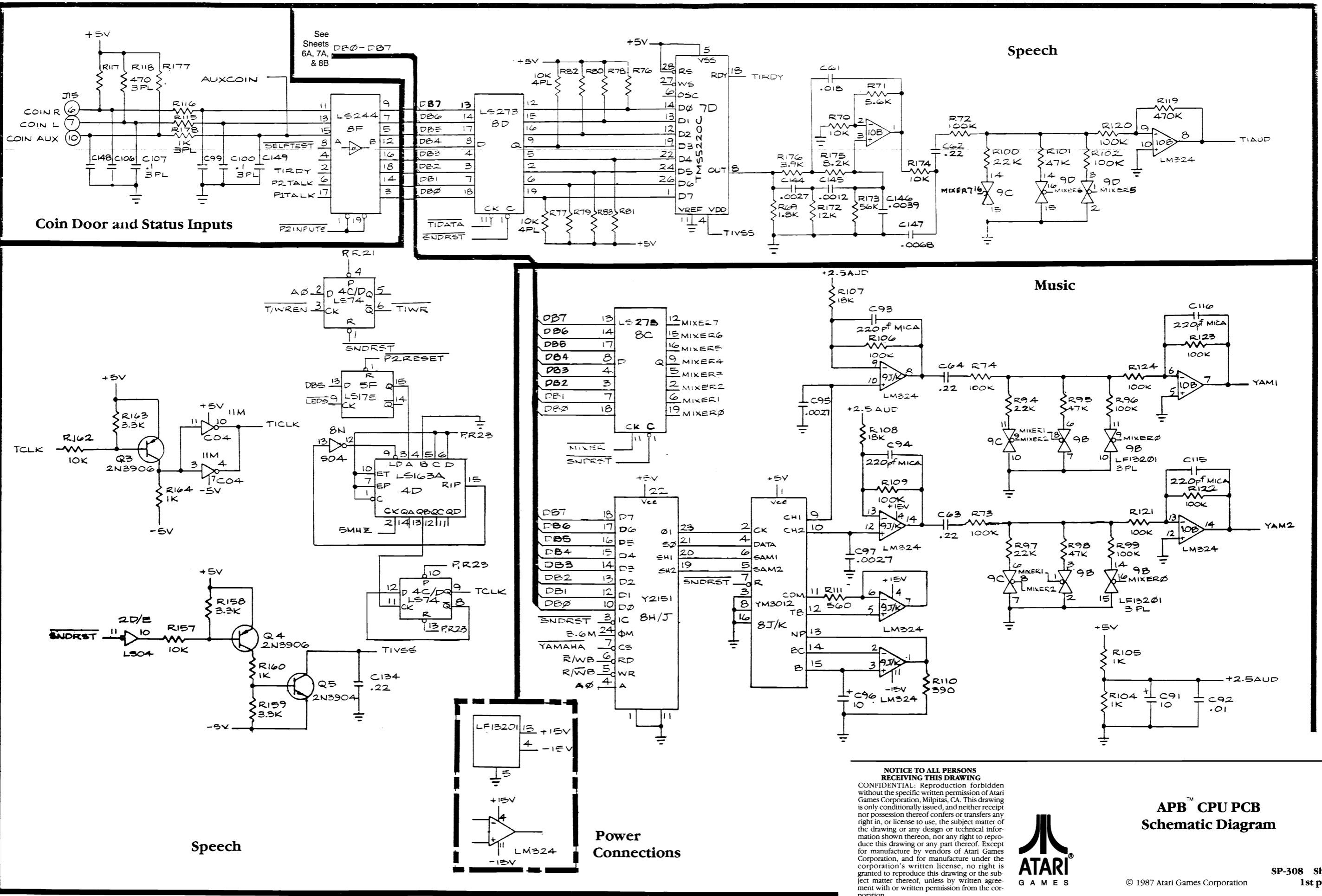


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APB™ CPU PCB Schematic Diagram





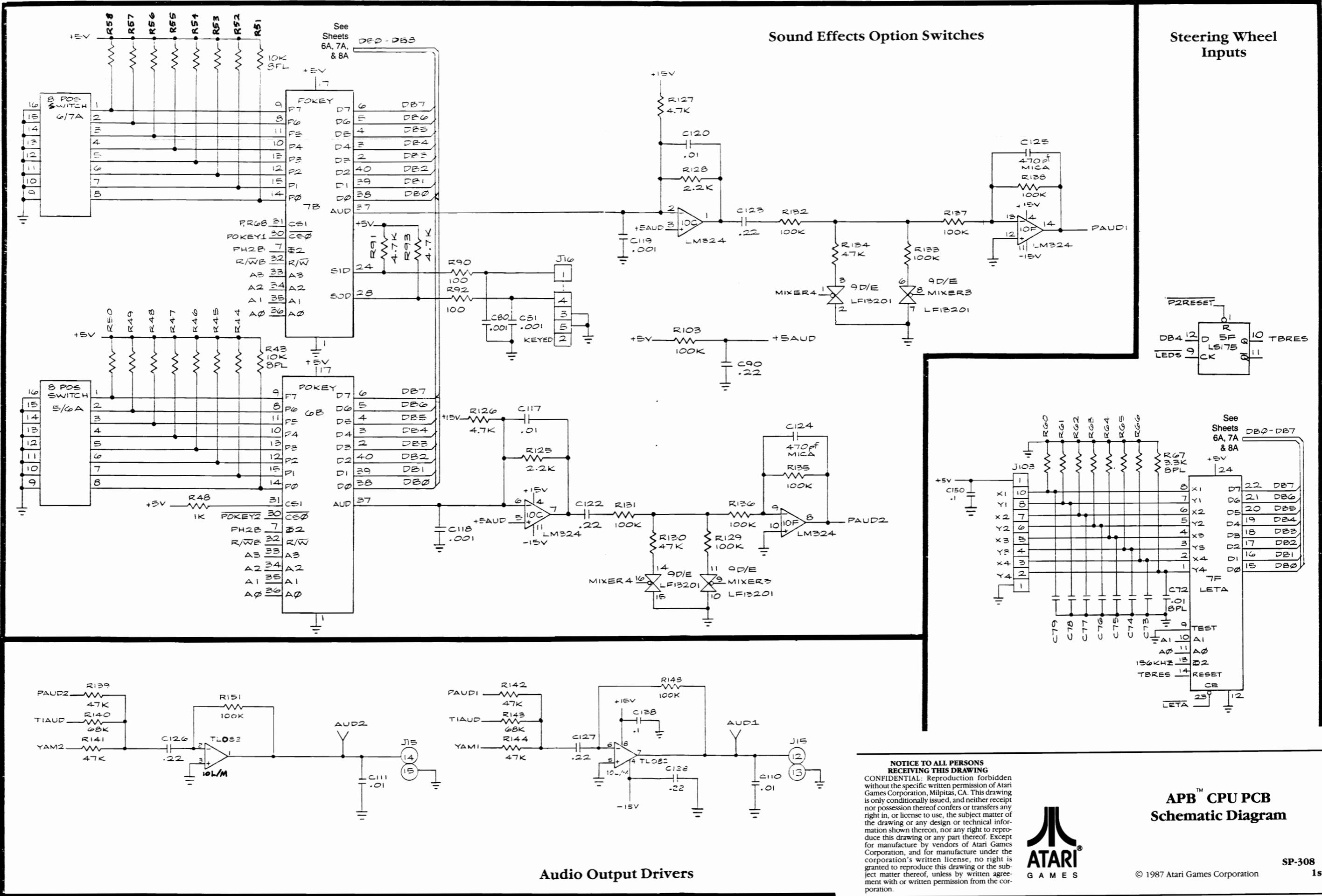
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APB™ CPU PCB
Schematic Diagram



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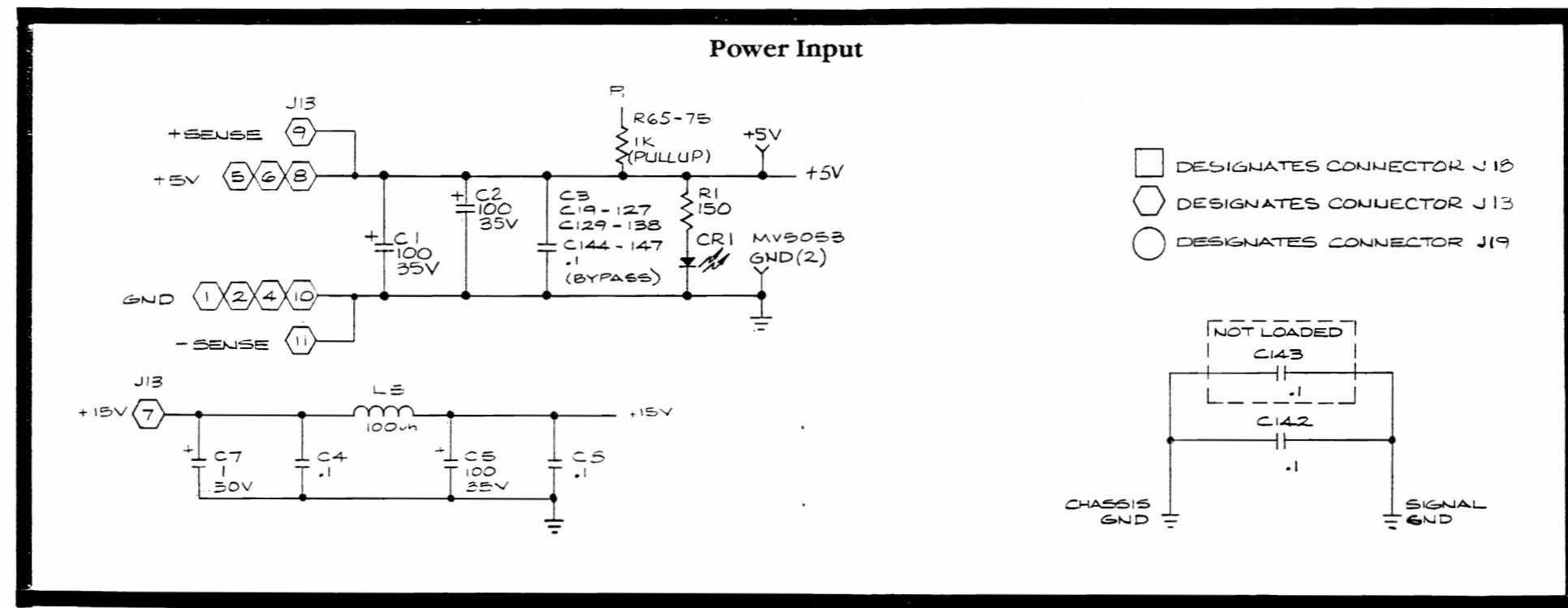
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**APB™ CPU PCB
Schematic Diagram**



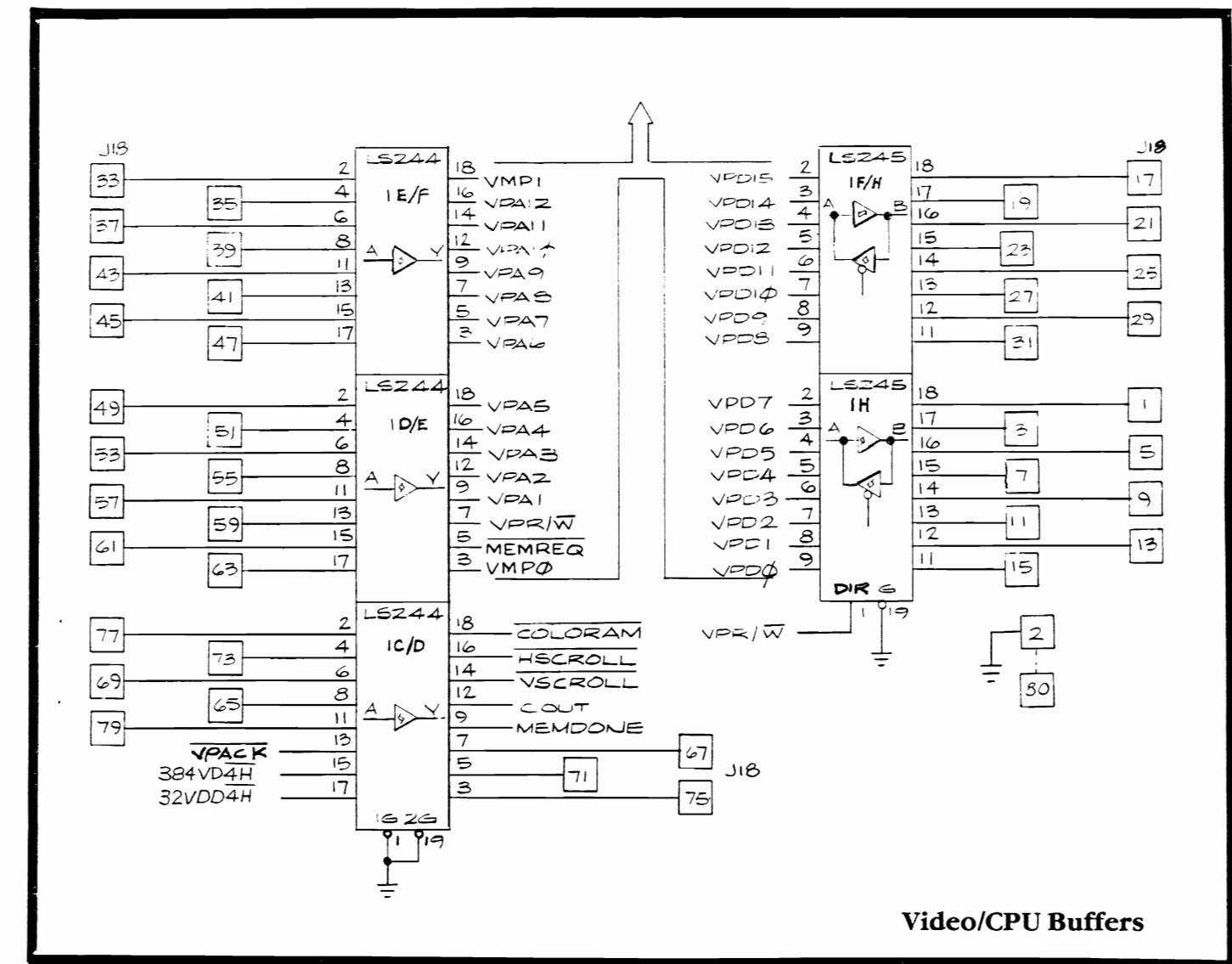
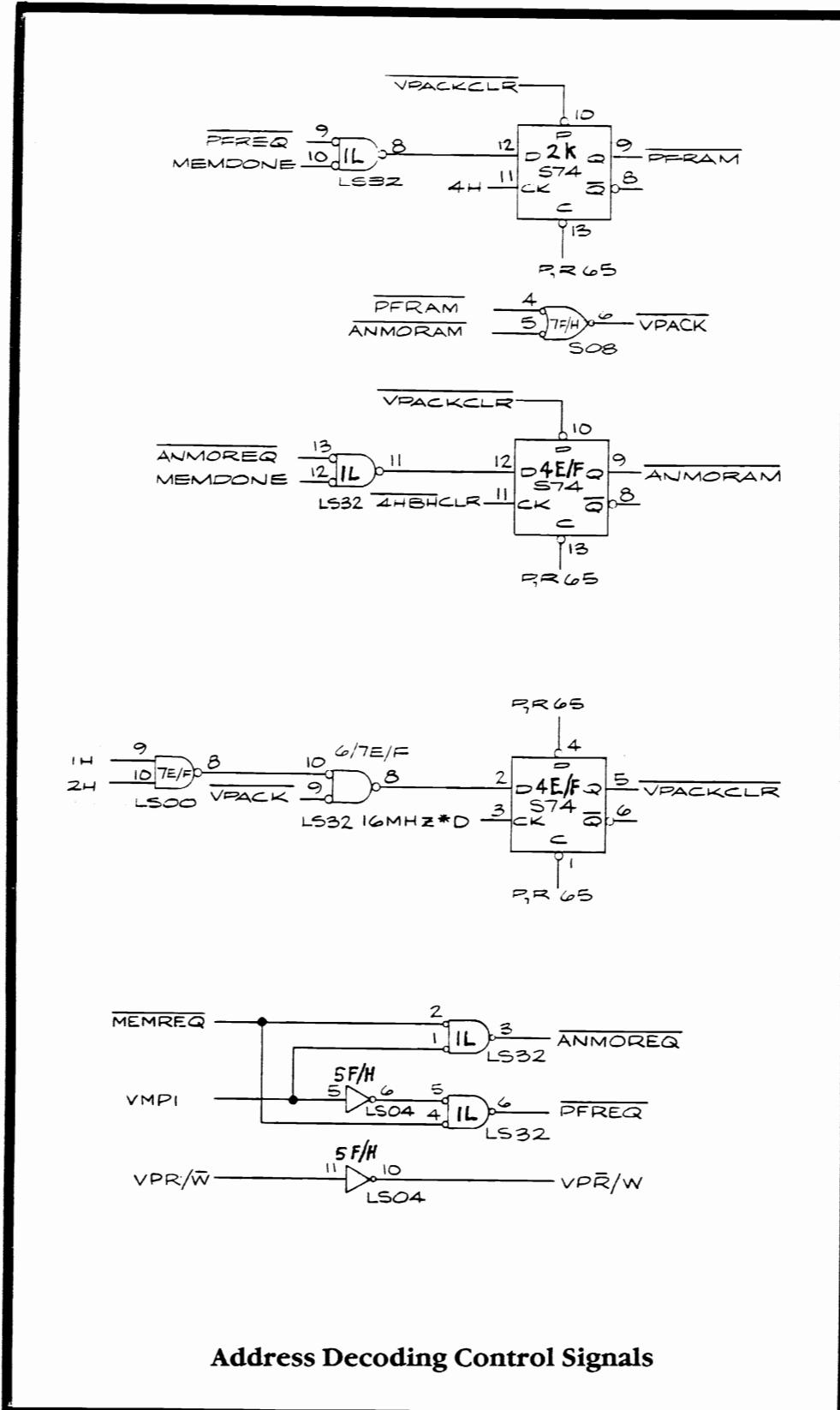
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APBTM Video PCB Schematic Diagram



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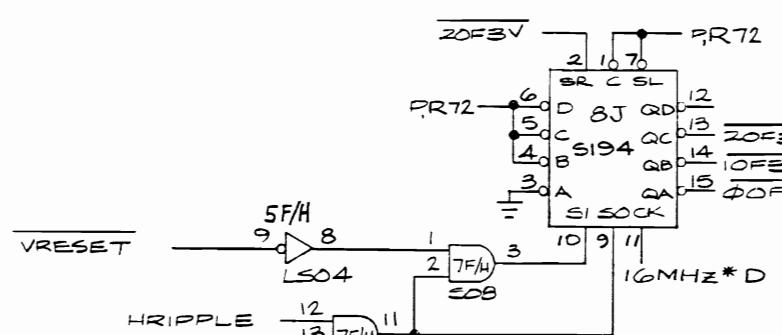
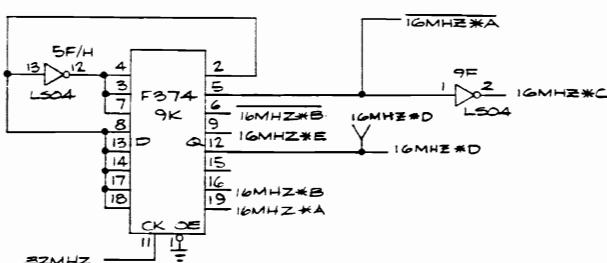
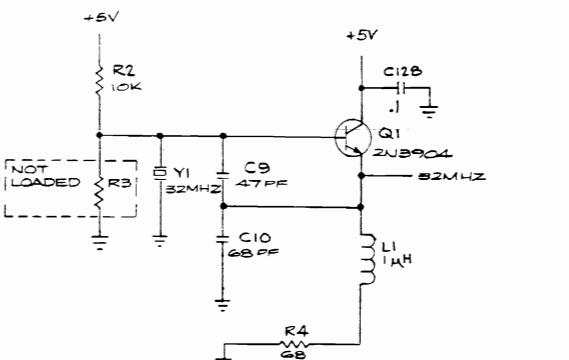
APB™ Video PCB Schematic Diagram



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1st printing

Video Clock



NIBLOAD*B WORD 500

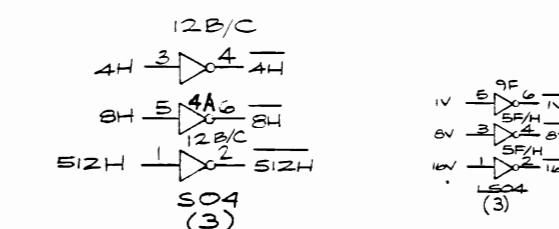
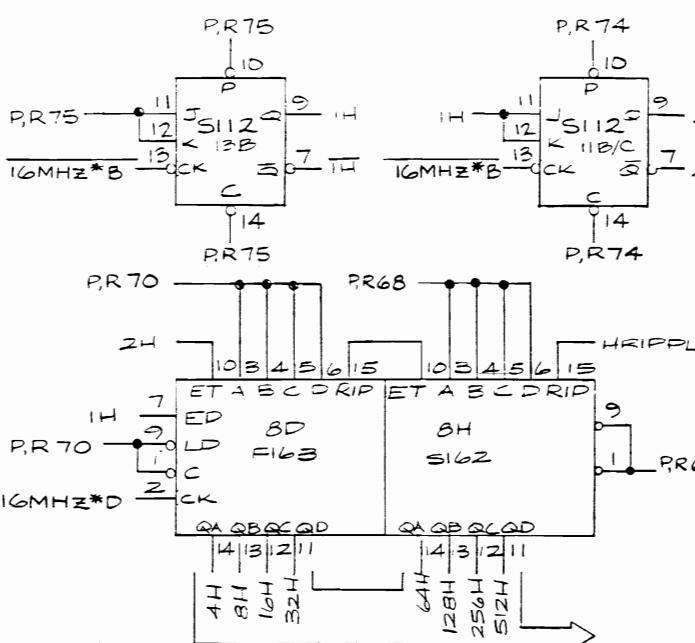
4HSH NIBLOAD*B 512H FIRSTWORD 512HD16H

20F3V 10 9 8 MOHLDΦ

10F3V 1 2 11 MOHLDI LS32

10F3V 12 13 11 MOHLD2 LS32

WORD 12 13 2T MOHLDIS LS32



NIBLOAD*B 10B/C 4H

5B/C 8H 12B/C 512H

500 16V 32V 64V

LS08 (3)

20F3V 10 8 BYTEL0 4H

5B/C 10 8 5B/C 500

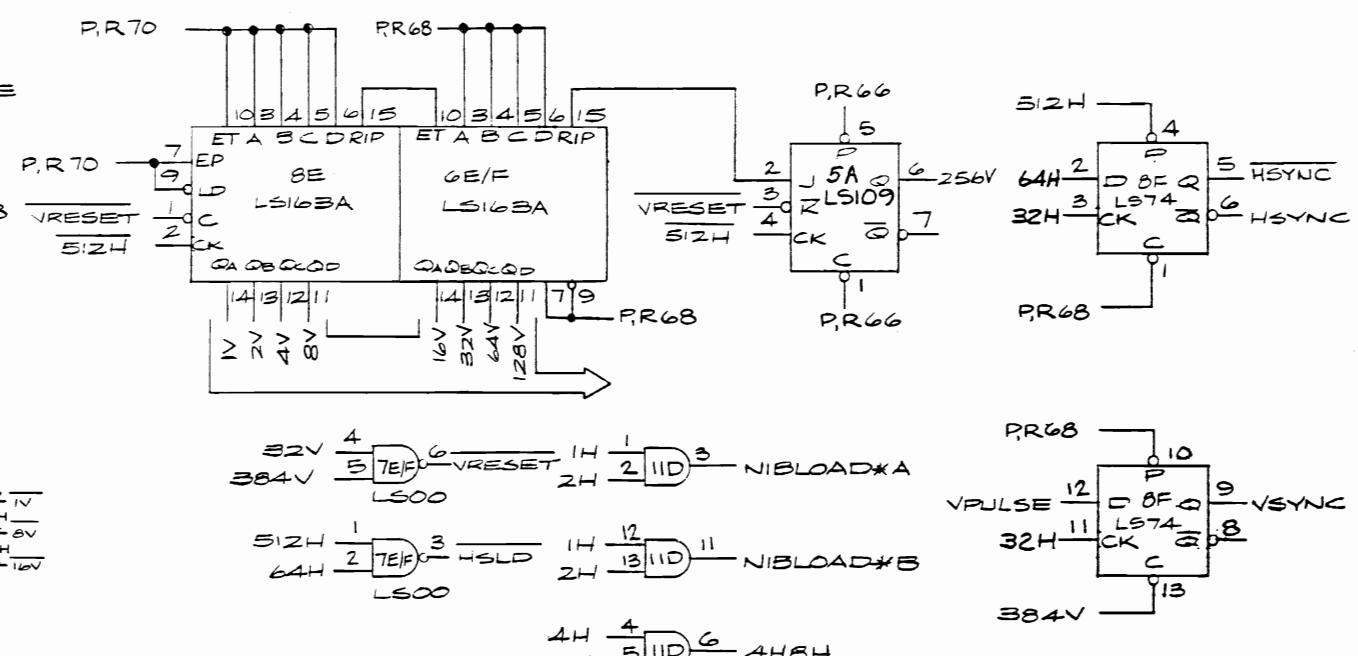
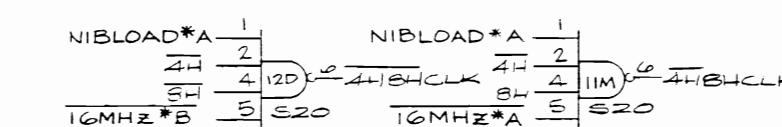
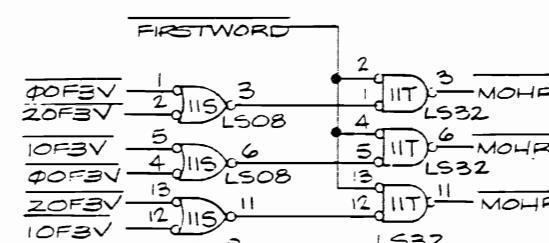
16V 10 8 256V 384V

LS08

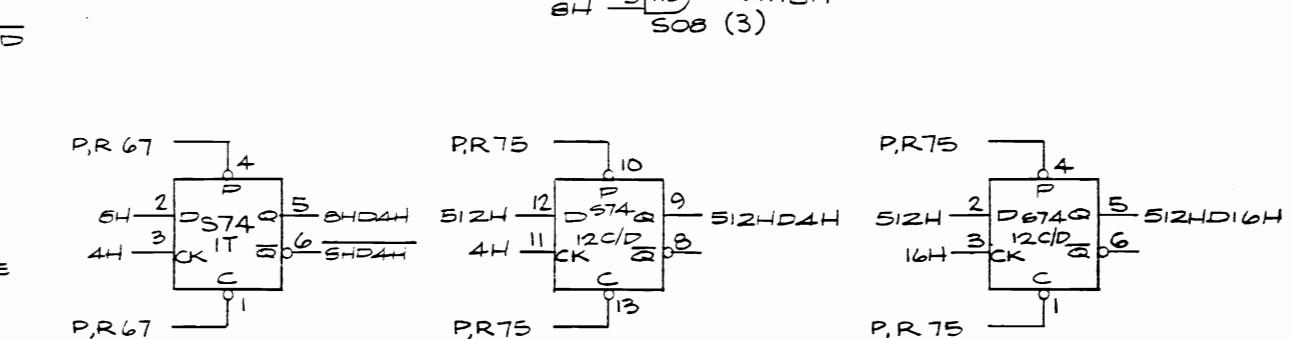
16V 1 2 3 VPULSE

5B/C 12 11 LS08

4V 12 13 LS08



Sync Chain and Timing Strobes

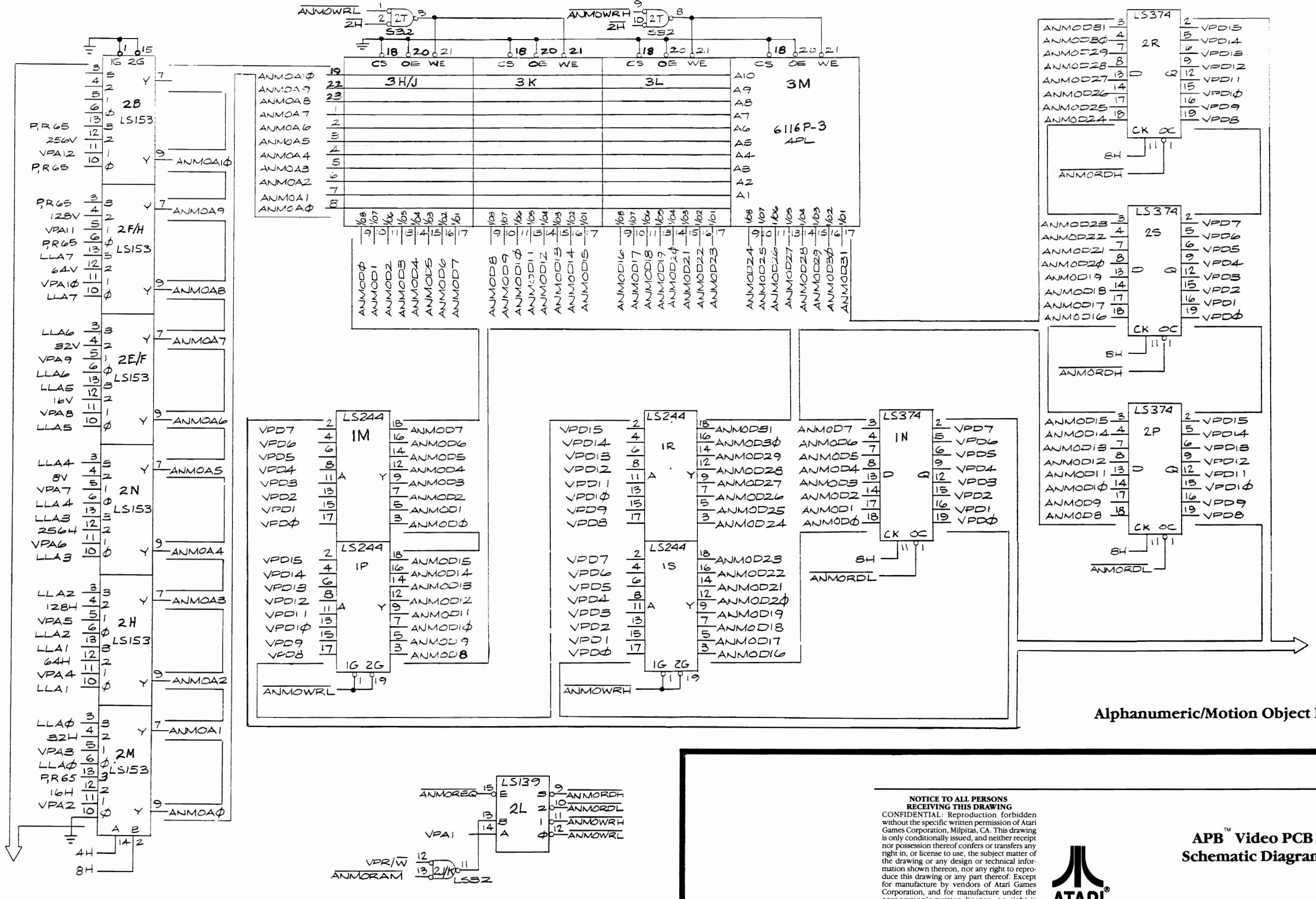


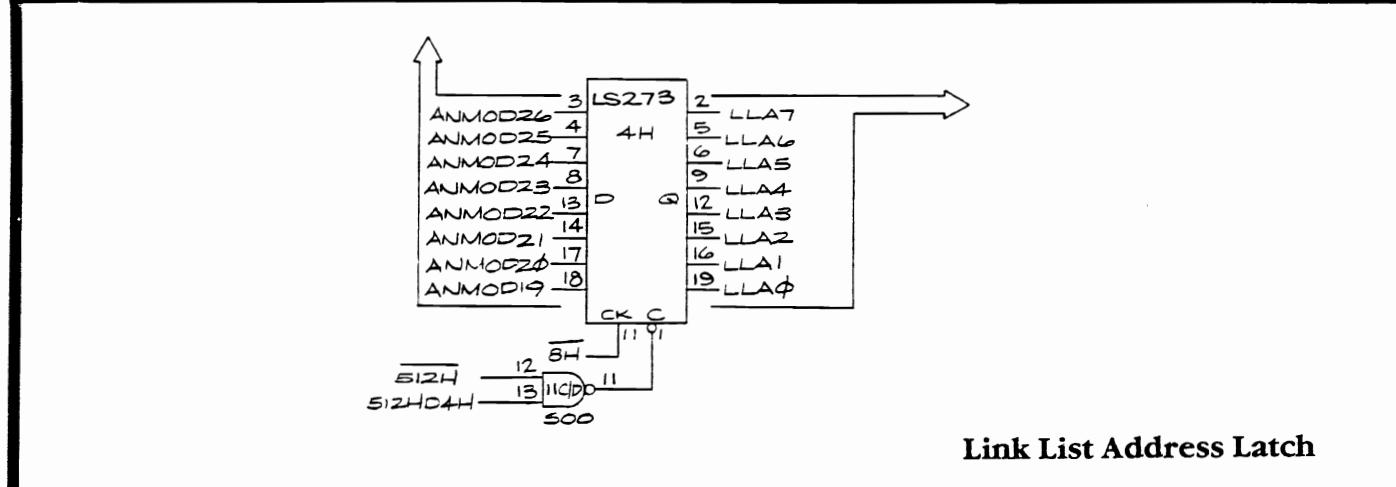
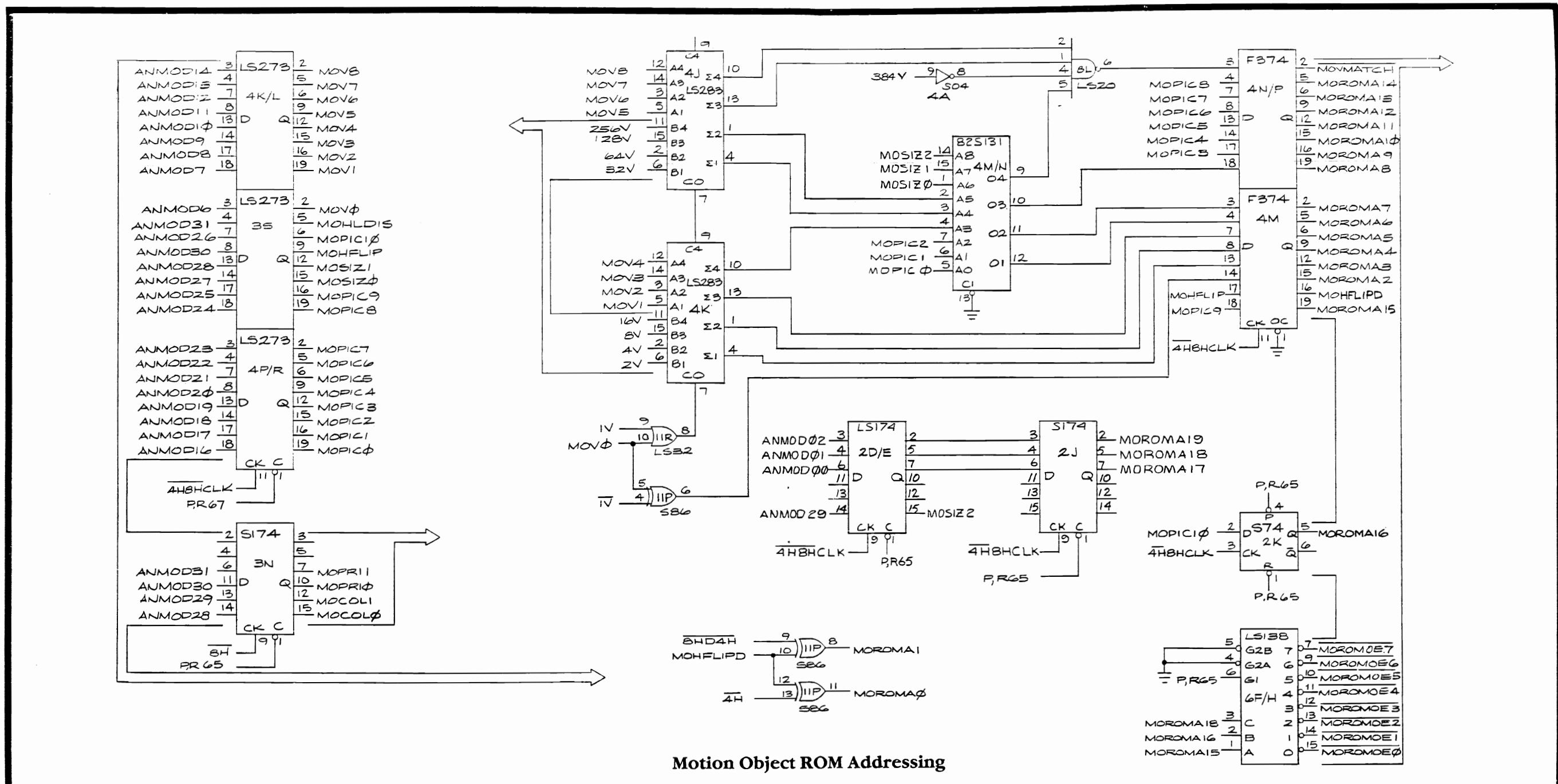
1H 13 12 BLNKCLK
2H 2 12 1 S10

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APB™ Video PCB Schematic Diagram





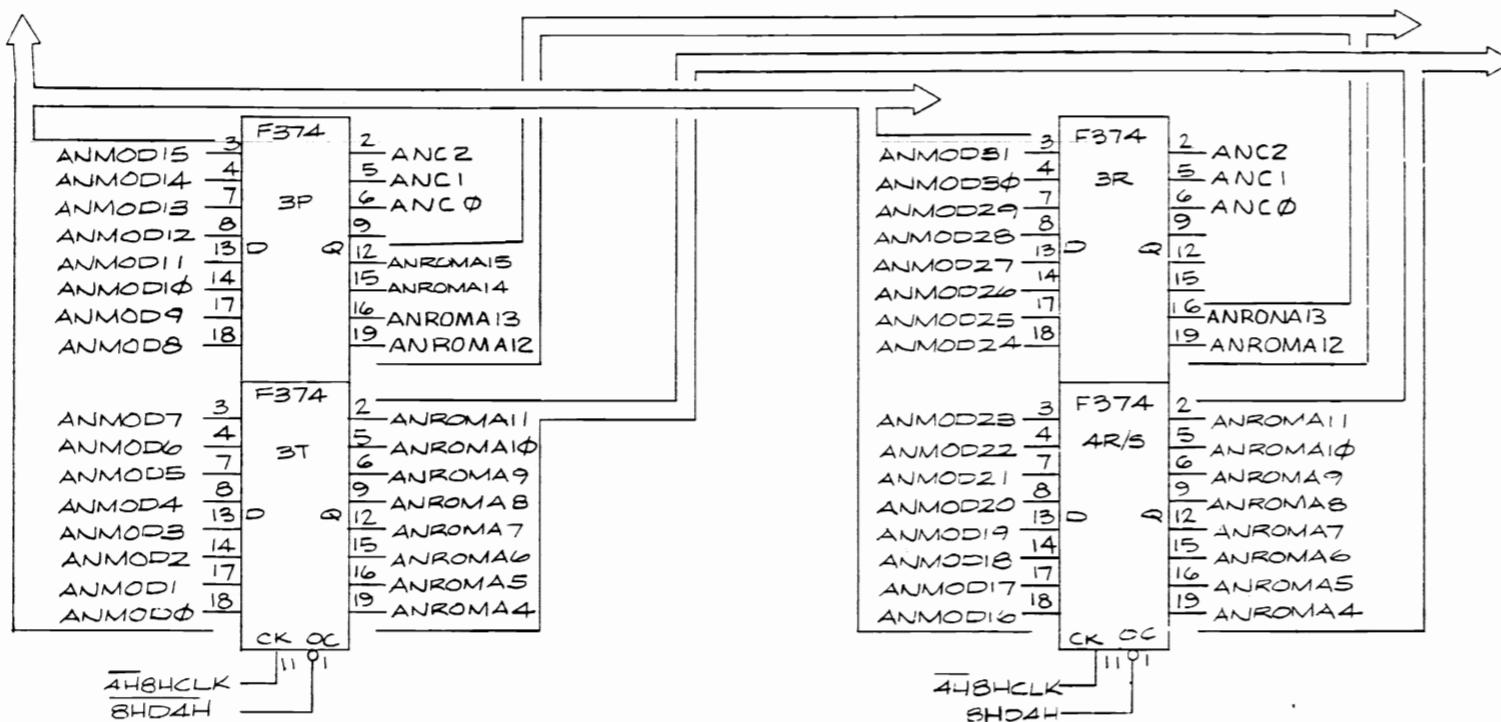
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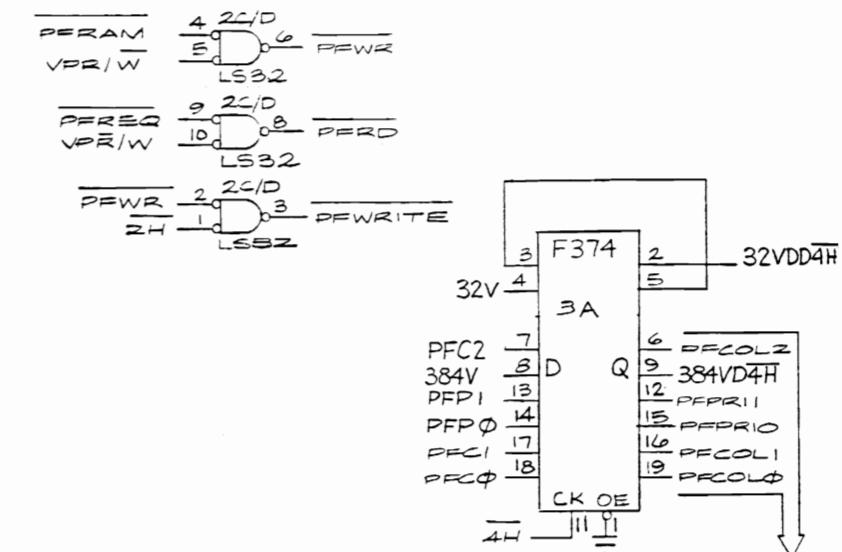
**APB™ Video PCB
Schematic Diagram**

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Alphanumeric ROM Addressing



Playfield Data Latch Strobes



Block diagram showing connections between logic blocks (PFB03-PFB01, PFB00-PFB10) and external components (S157, PFBS3, PFBS2, PFBS1, PFBS0, output 14). The connections are summarized below:

- Section A (PFB03-PFB01):** PFB03 connects to S157, PFBS3, and PFBS2. PFB02 connects to S157, PFBS3, and PFBS2. PFB01 connects to S157, PFBS3, and PFBS2.
- Section B (PFB00-PFB10):** PFB00 connects to S157, PFBS2, and PFBS1. PFB01 connects to S157, PFBS2, and PFBS1. PFB02 connects to S157, PFBS1, and PFBS0. PFB03 connects to S157, PFBS0, and output 14.
- Bus Connections:** The bus connects to S157, PFBS3, PFBS2, PFBS1, PFBS0, and output 14.

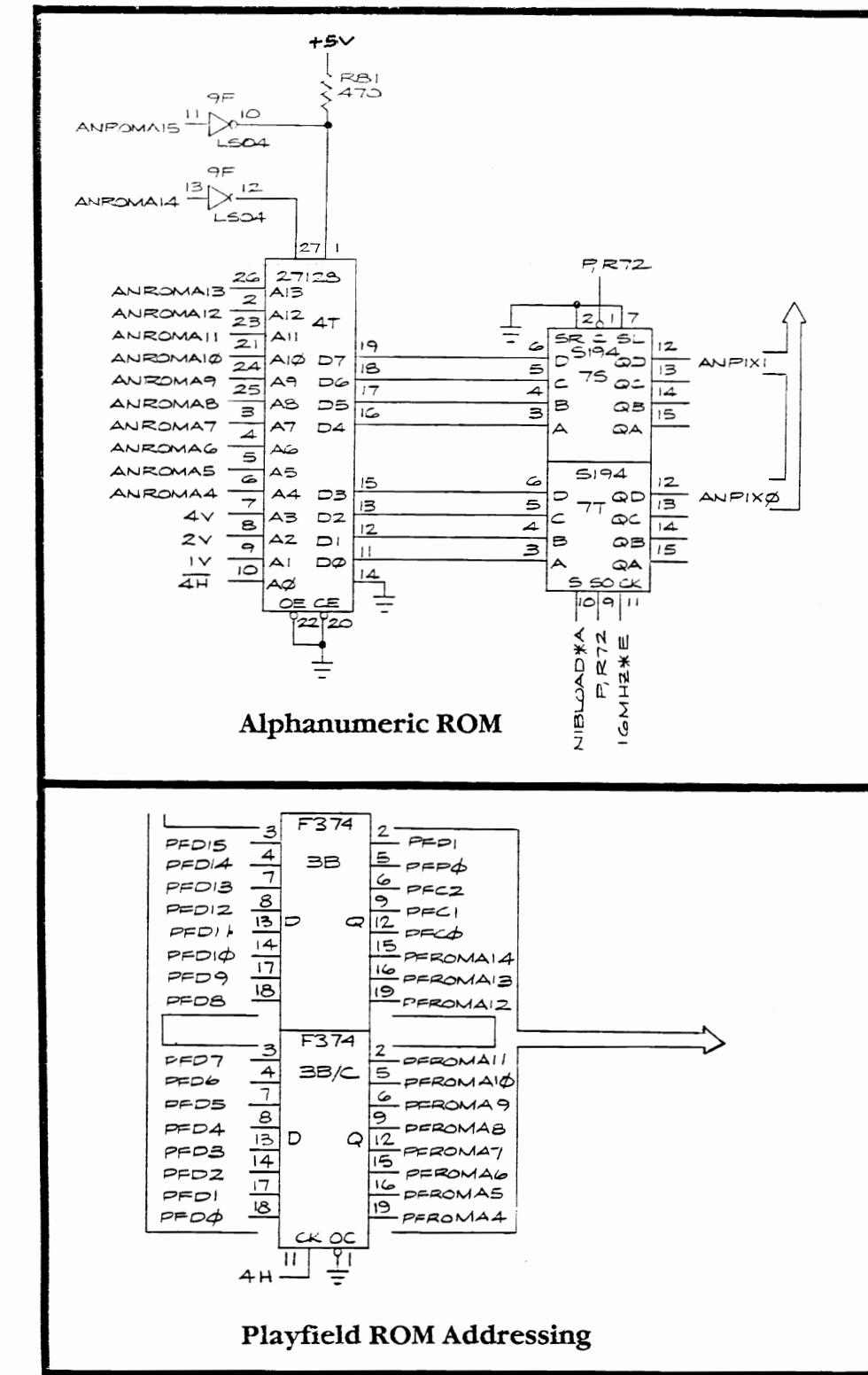
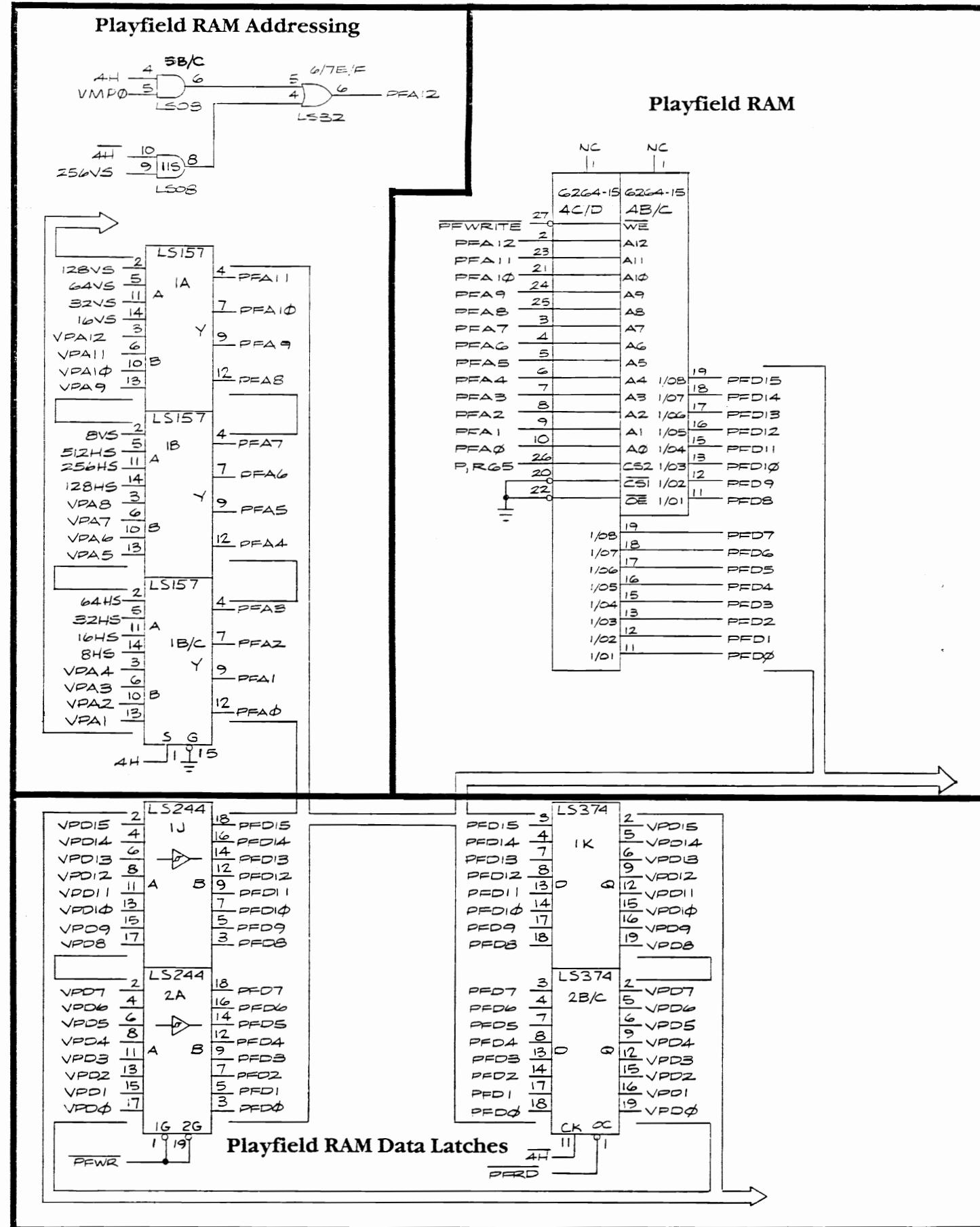
Playfield Bank Select

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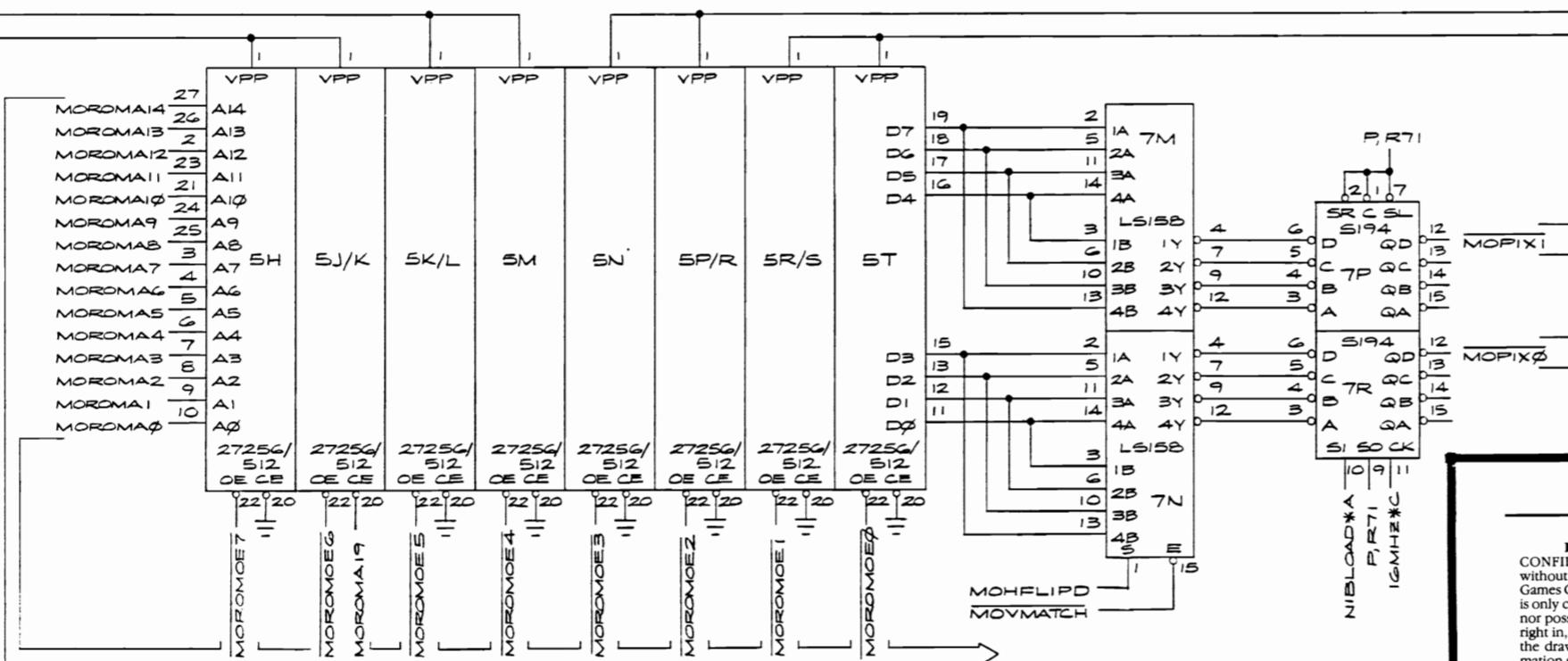
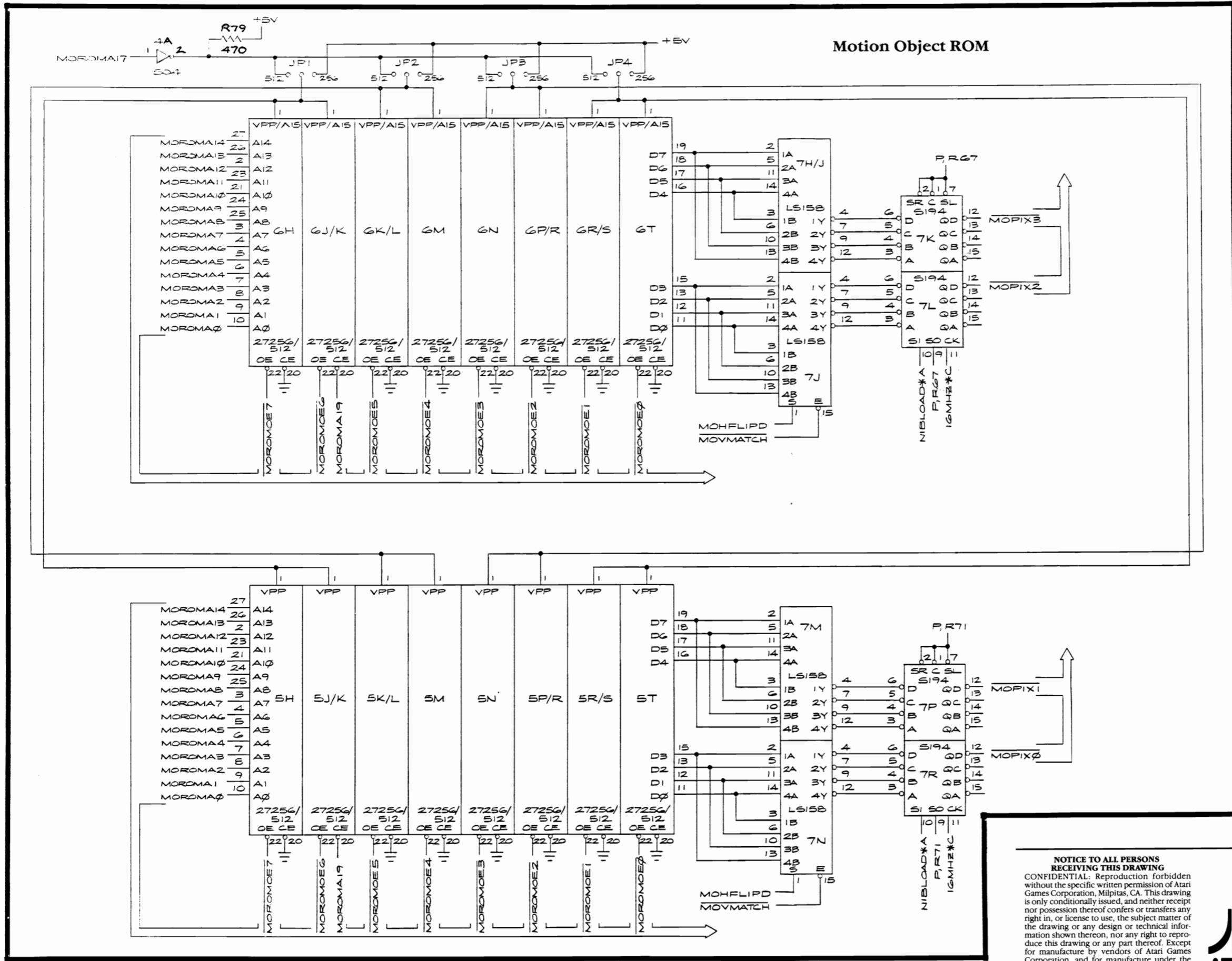
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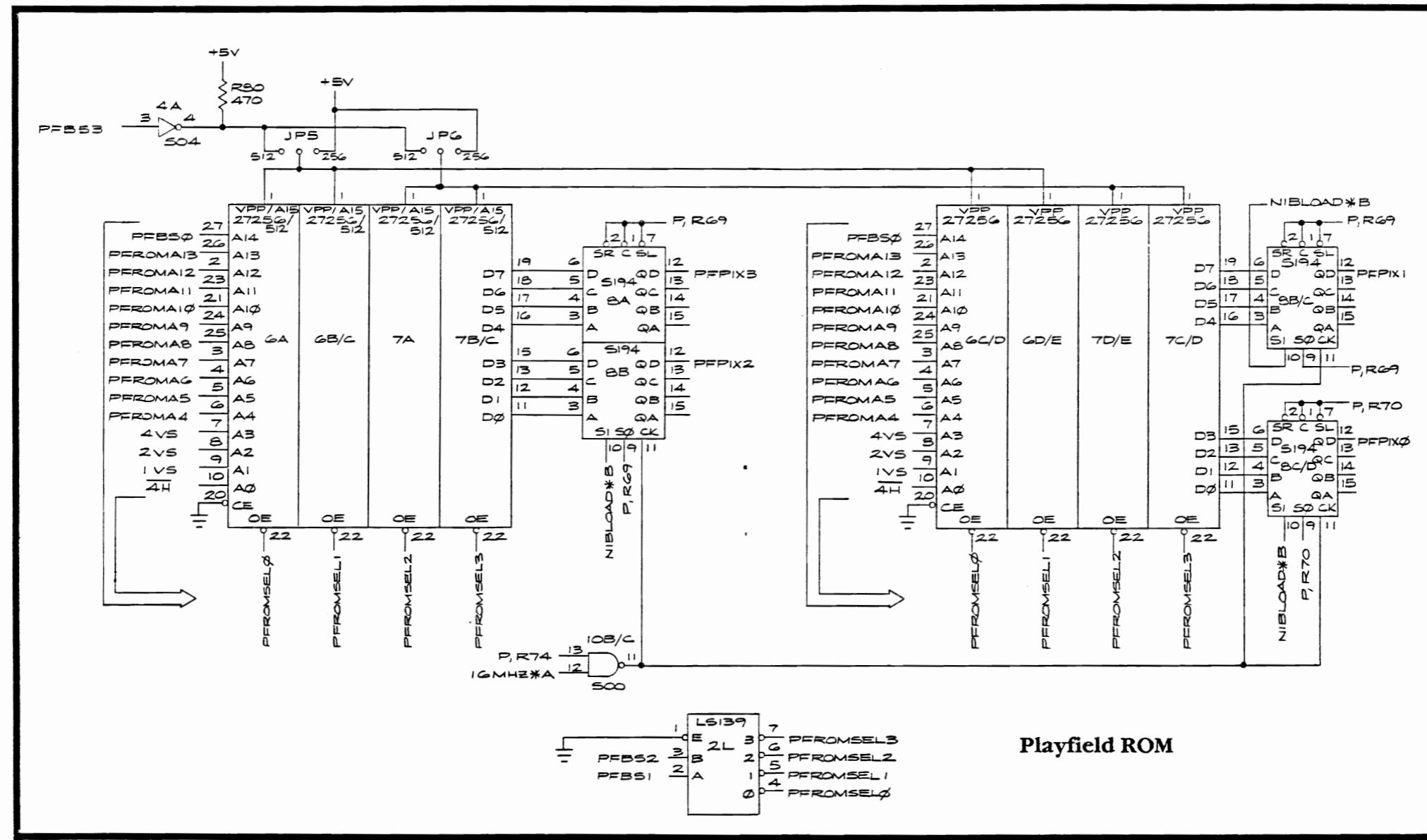
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**APB™ Video PCB
Schematic Diagram**

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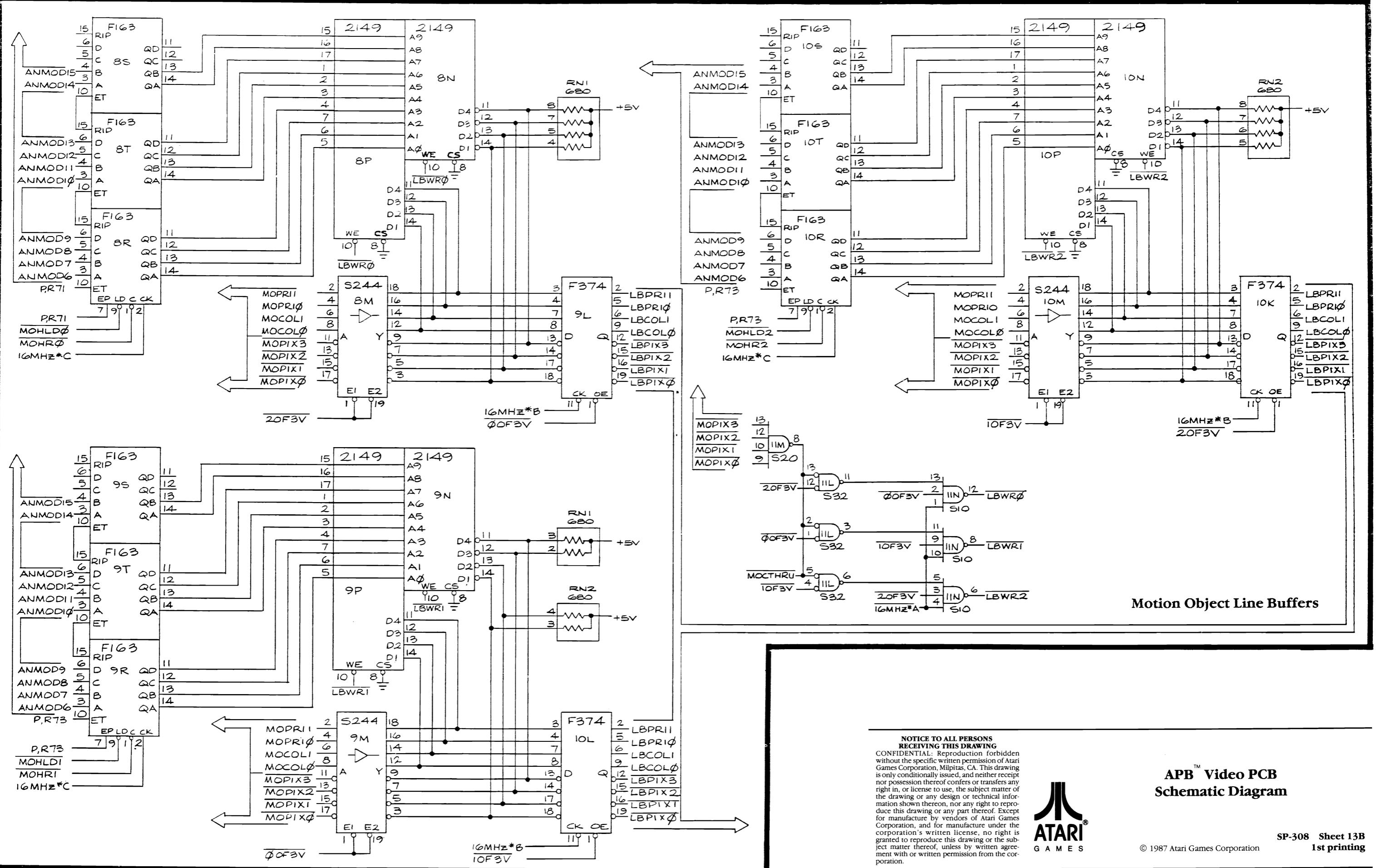
Playfield ROM

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APBTM Video PCB Schematic Diagram



Motion Object Line Buffers

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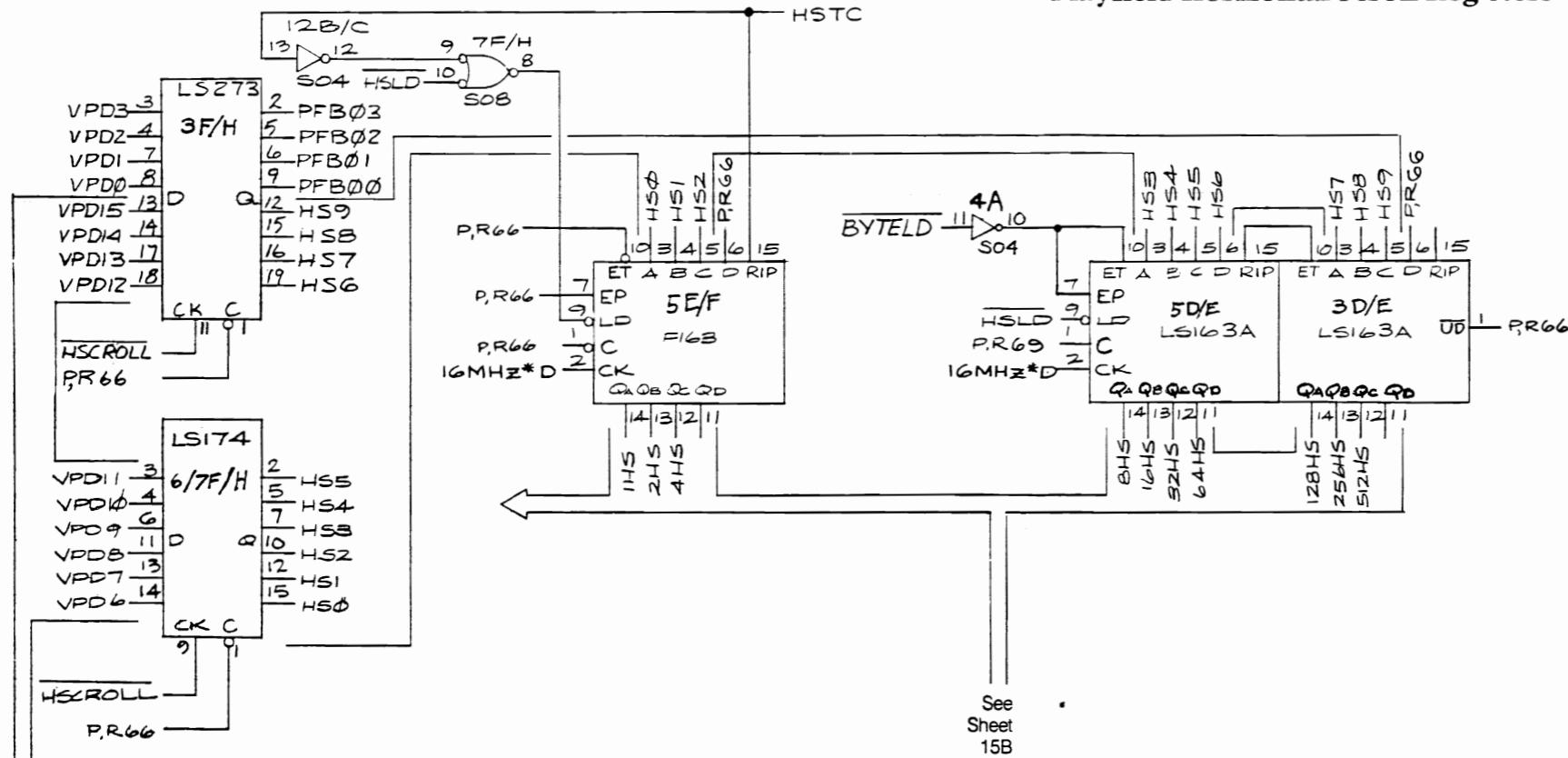
**APB™ Video PCB
Schematic Diagram**



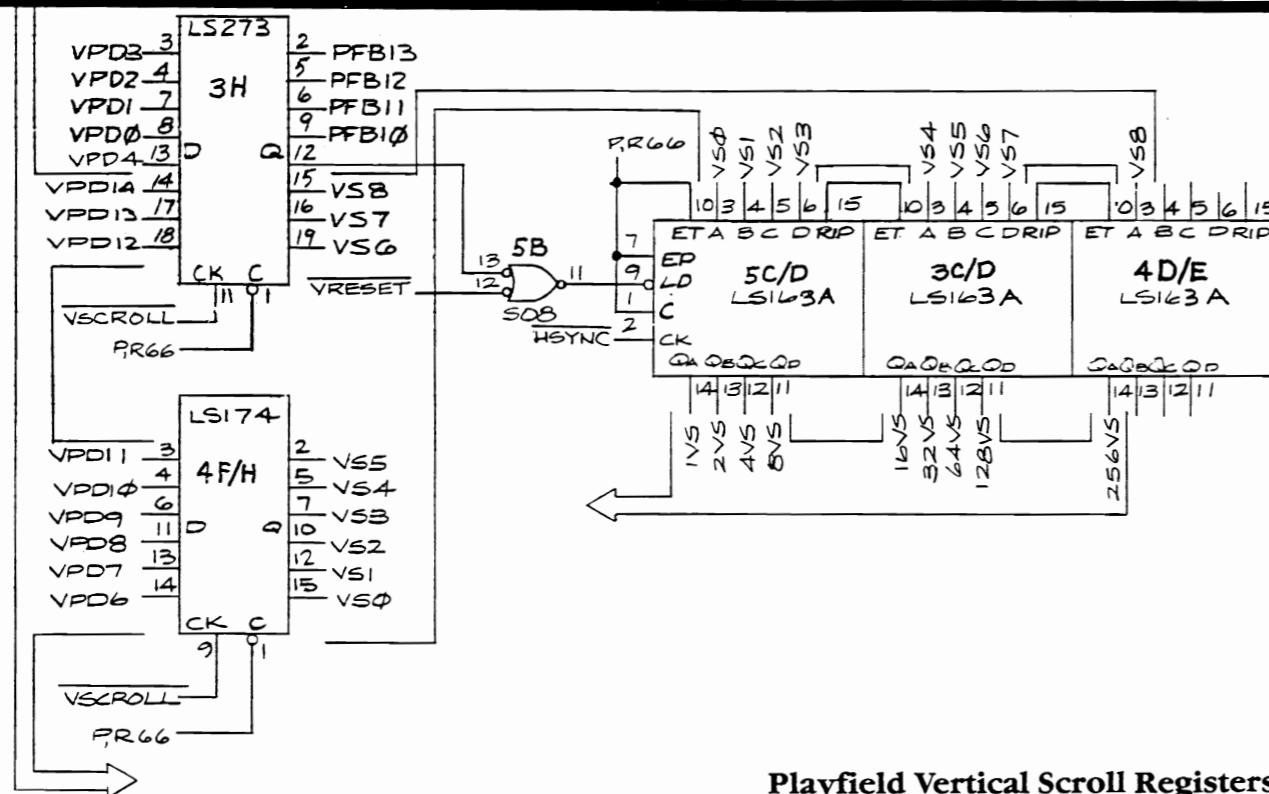
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Playfield Horizontal Scroll Registers



Playfield Vertical Scroll Registers

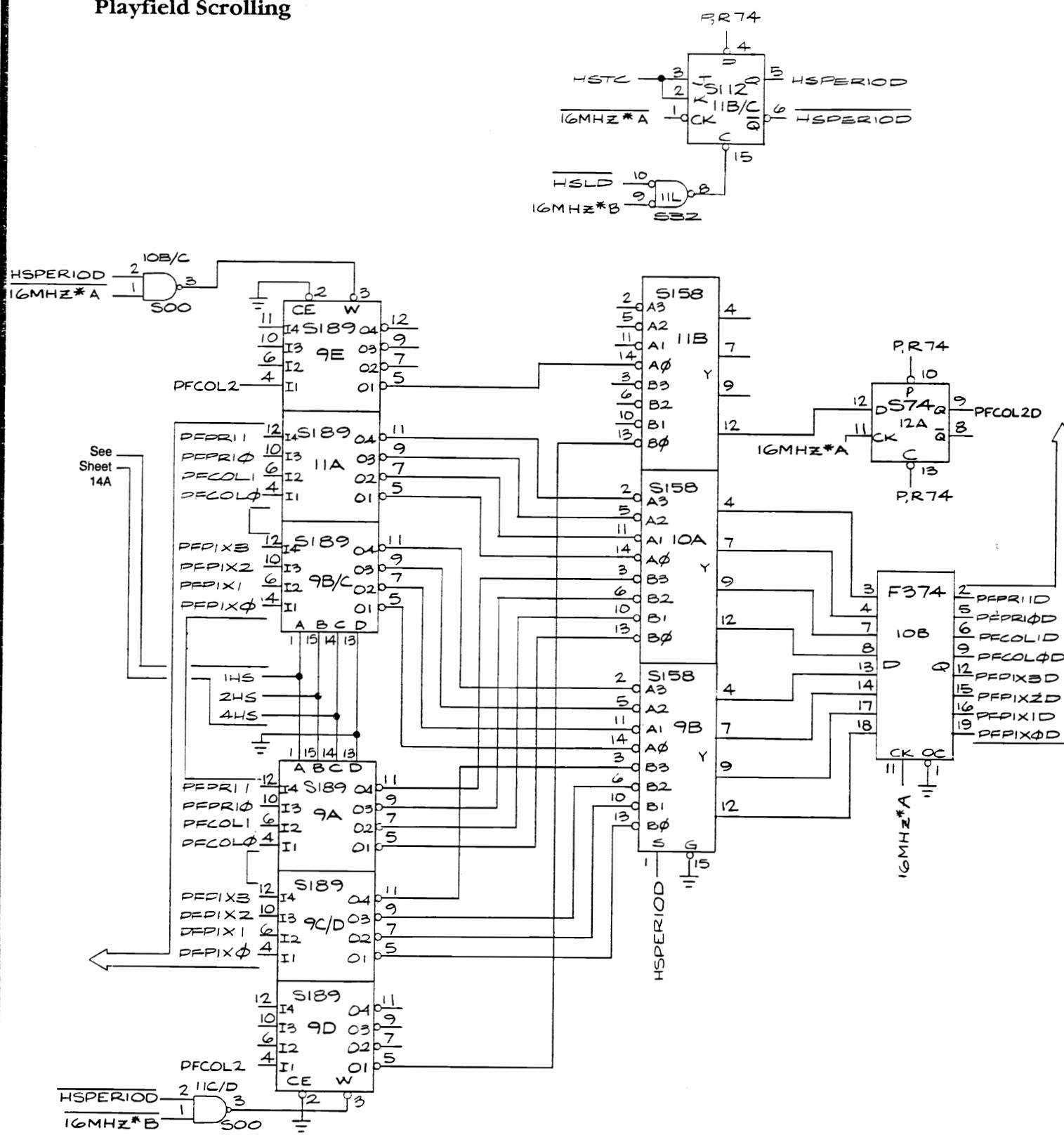


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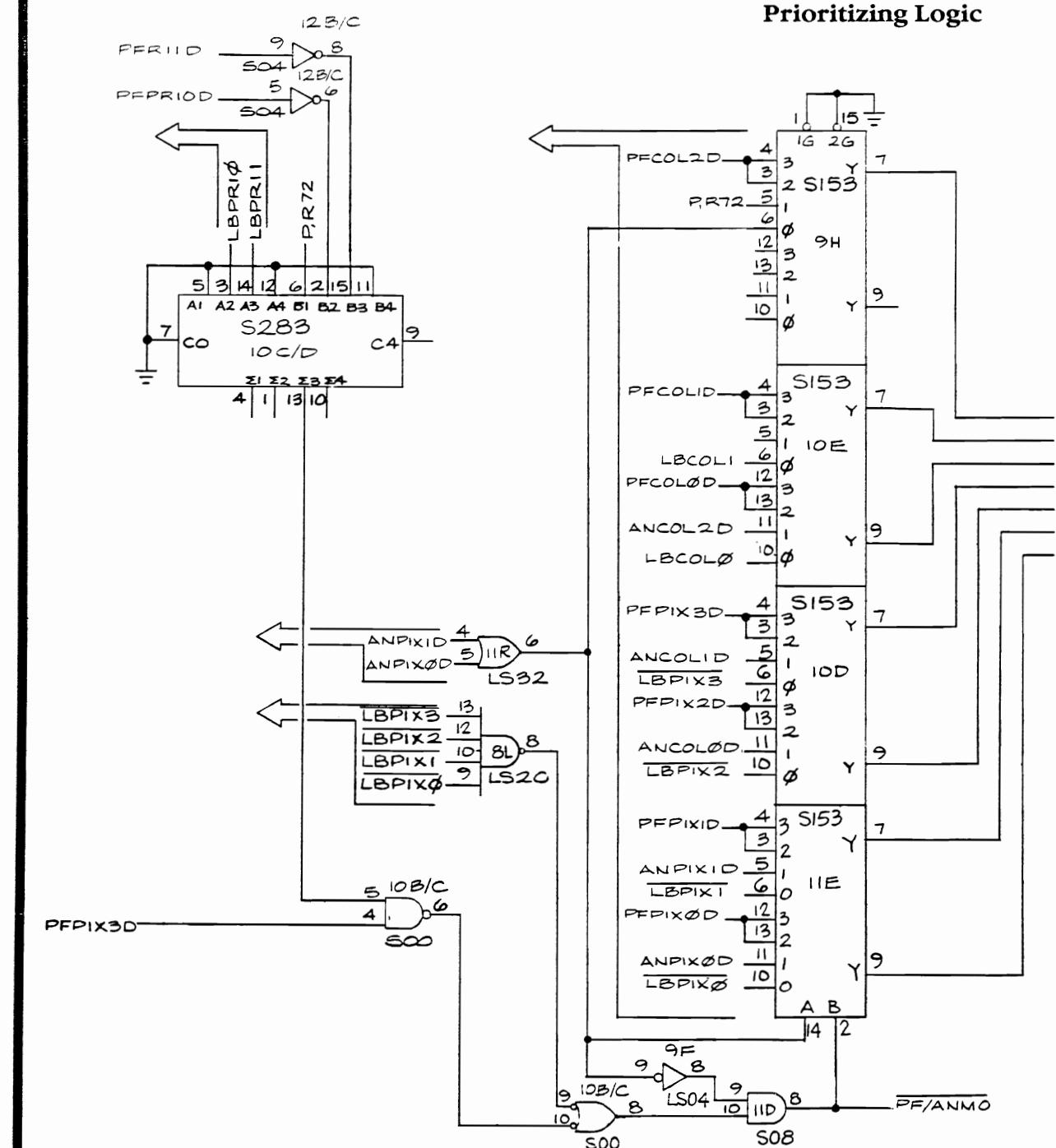
APB™ Video PCB Schematic Diagram



Playfield Scrolling



Prioritizing Logic

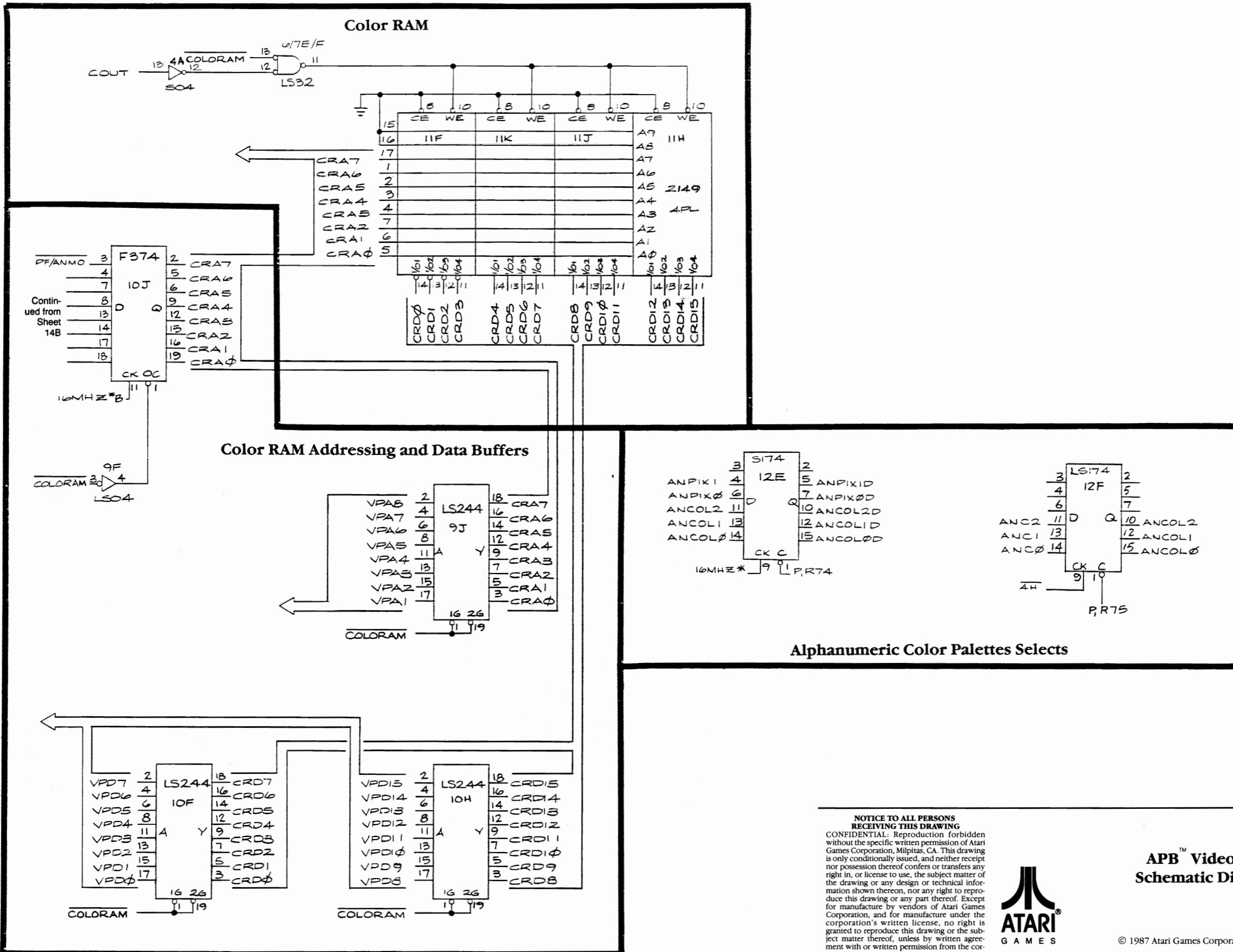


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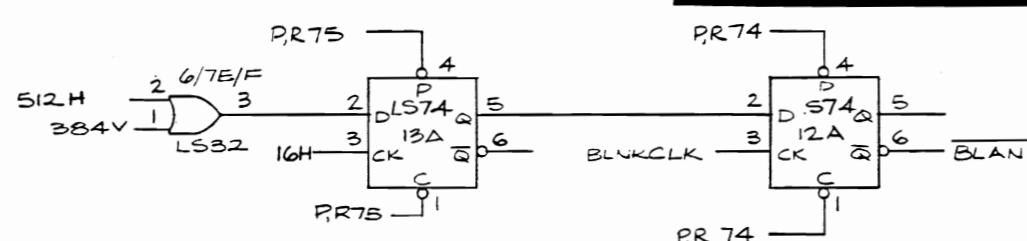
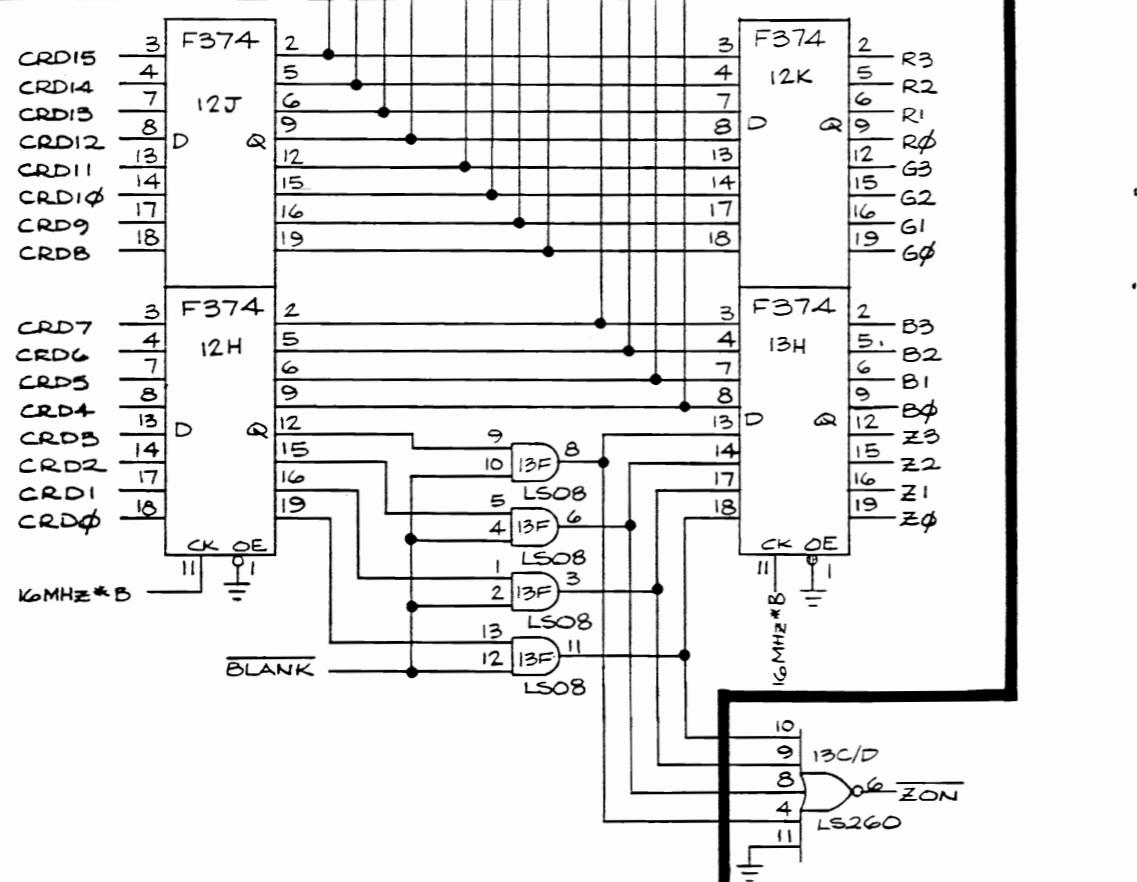
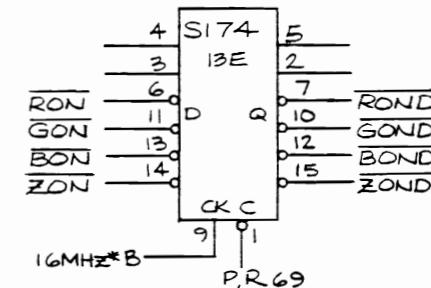
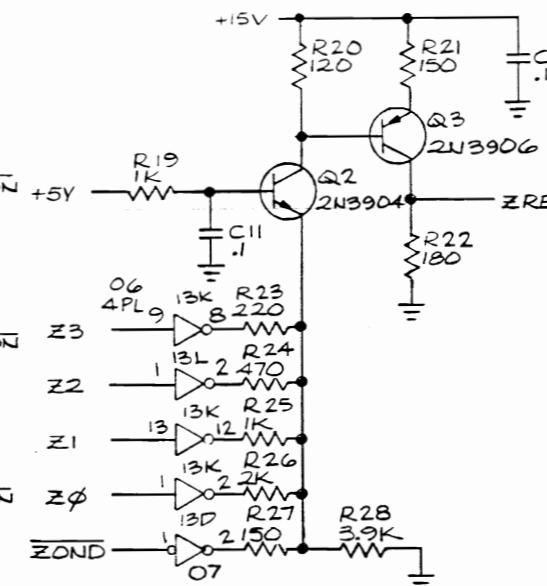
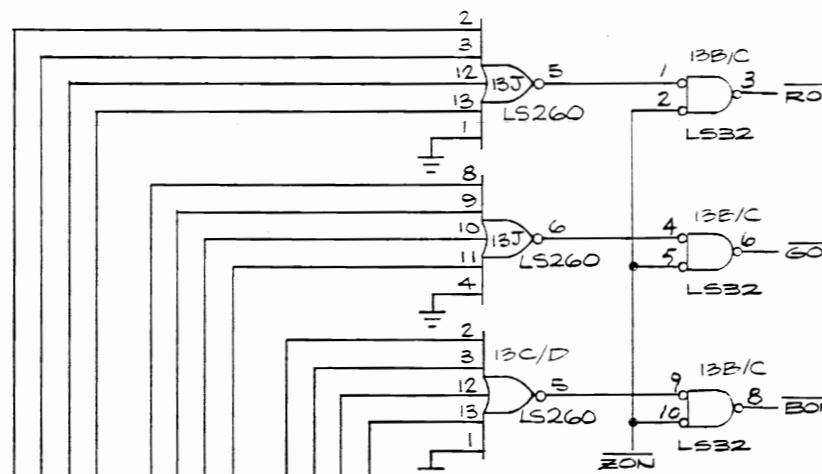
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**APB™ Video PCB
Schematic Diagram**



Video Intensity Control and Driver Enables



Data Latches and Blanking

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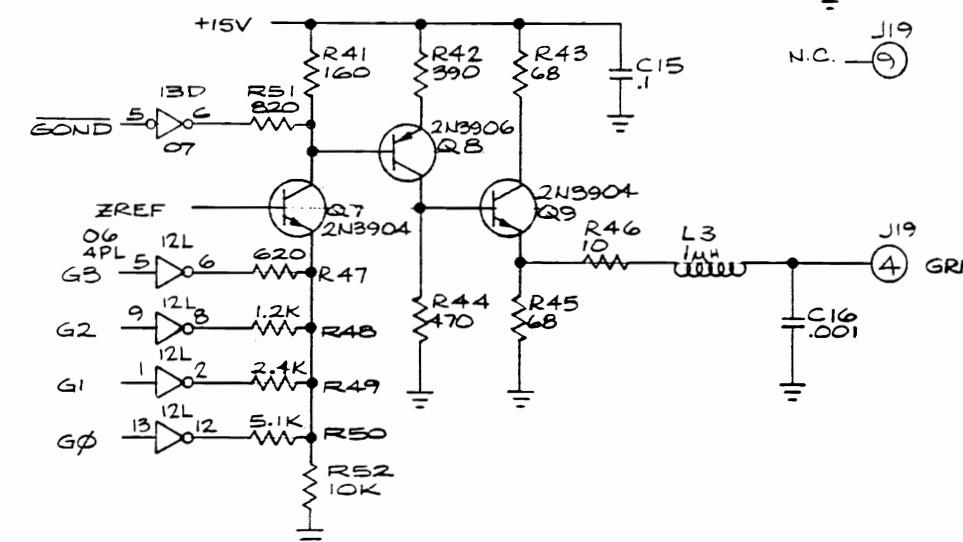
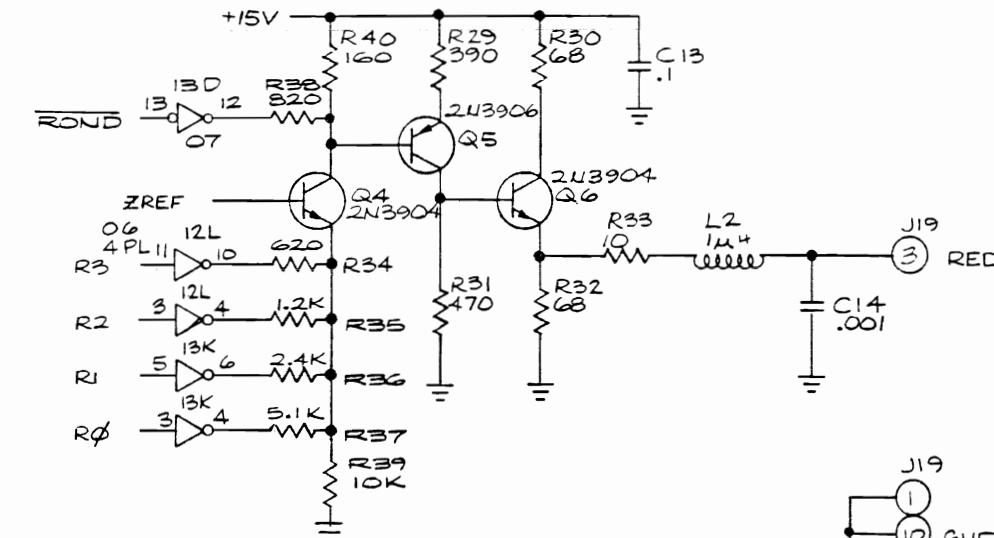
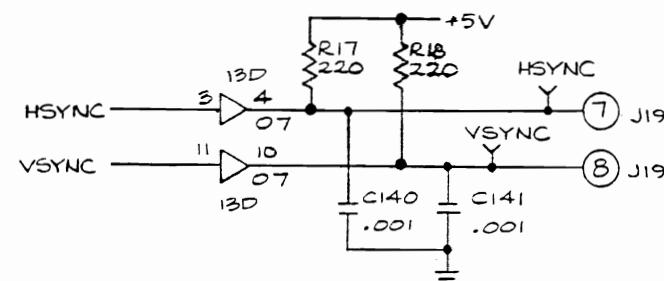
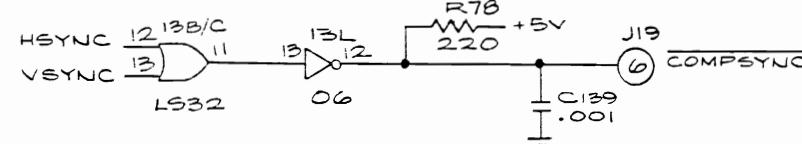
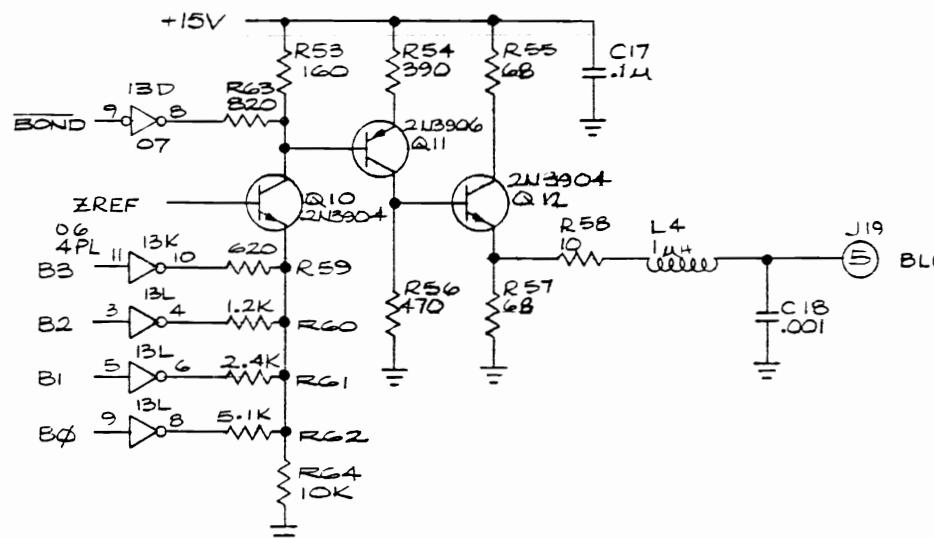
**APB™ Video PCB
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Output Drivers



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APBTM Video PCB Schematic Diagram

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